WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

400G QSFP112 DR4 500 m Transceiver Module
P/N: WST-Q112-DR4-C

Features:

- 400G QSFP112 DR4 optical transceiver module
- Supports aggregate data rate up to 425 Gb/s
- Four electrical lanes at 106.25 Gb/s PAM4 per lane
- Four optical lanes at 106.25 Gb/s PAM4 per lane
- 53.125 GBd PAM4 signaling rate
- 1310 nm silicon photonics optical engine
- Transmission distance from 2 m to 500 m over G.652 SMF with FEC
- MPO-12/APC optical interface
- Single +3.3 V power supply
- Maximum power consumption: 10 W
- Digital diagnostic monitoring functions supported
- Operating case temperature: 0 °C to 70 °C
- RoHS compliant

Application:

- 400G Ethernet interconnects
- Data center interconnects
- Switch-to-switch and switch-to-router interconnects
- Medium-reach optical transmission over single-mode fiber

Standard:

- Compliant with IEEE 802.3cn
- Compliant with IEEE 802.3ck
- Compliant with QSFP112 Multi-Source Agreement (MSA)
- Management interface compliant with CMIS 5.2 or later

Description

The WST-Q112-DR4-C is a 400G QSFP112 DR4 optical transceiver module designed for medium-reach data communication and interconnect applications over single-mode fiber. It supports an aggregate data rate of 425 Gb/s and transmission distance from 2 m to 500 m over G.652 SMF with FEC. The module uses a 1310 nm silicon photonics optical engine and provides a 4-lane optical interface through an MPO-12/APC connector.

Function Description:

The module provides four electrical lanes and four optical lanes operating at 106.25 Gb/s PAM4 per lane. The electrical interface is compliant with 400GAUI-4 requirements and supports a 53.125 GBd PAM4 signaling rate. The module integrates internal control and management functions and supports digital diagnostic monitoring through a CMIS 5.2 or later management interface. It operates from a single +3.3 V power supply with a maximum power consumption of 10 W and supports commercial case temperature operation from 0 °C to 70 °C.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_S	-40		85	°C	
Relative Humidity	RH	5		85	%	Non-condensing
Damage Threshold, each lane				5	dBm	1

Note1:

The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Electrical Signal Rate, each lane		53.125 ± 100 ppm			GBd	
Optical Signal Rate, each lane		53.125 ± 100 ppm			GBd	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Operating Case Temp.	Tc	0		70	°C	
Power Consumption	Pc		9	10	W	
Link Distance with G.652	Dl	2		500	m	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
High Speed Electrical Input Characteristics						
Signaling rate per lane (PAM4 encoded)	TP1	-100 ppm	53.125	+100 ppm	GBd	
Differential peak-peak input voltage tolerance	TP1a	750			mV	
AC common-mode RMS voltage tolerance	TP1a	25			mV	
Single-ended voltage tolerance	TP1a	-0.4		3.3	V	
DC common-mode voltage	TP1	-0.35		2.85	V	
High Speed Electrical Output Characteristics						

Signaling rate per lane (PAM4 Encoded)	TP4	-100 ppm	53.125	+100 ppm	GBd	
AC common-mode output voltage (RMS)	TP4			25	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	mV	
Eye height	TP4	15			mV	
DC common-mode voltage tolerance	TP4	-0.35		2.85	V	1

Note:

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling rate per lane (range)		-100 ppm	53.125	+100 ppm	GBd	
Modulation format			PAM4			
Lane wavelength (range)	λ	1304.5	1310	1317.5	nm	
Average launch power, each lane	P	-2.9		4	dBm	1
OMAouter, each lane	P_{OMA}	-0.8		4.2	dBm	2
Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.4	dB	
Side-mode suppression ratio (SMSR)		30			dB	
Extinction ratio, each lane	ER	3.5			dB	
Average launch power of OFF transmitter, each lane	P_{off}			-15	dBm	
RIN21OMA	RIN			-136	dB/Hz	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26	dB	3
Receiver						
Signaling rate per lane (range)		-100 ppm	53.125	+100 ppm	GBd	
Modulation format			PAM4			
Lane wavelength (range)	λ	1304.5	1310	1317.5	nm	
Damage Threshold, each lane		5			dBm	
Average receive power, each lane		-5.9		4	dBm	4
Receive power , each lane (OMAouter)	R_{OMA}			4.2	dBm	

Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane	SEN	max(-3.9, SECQ-5.3)			dBm	5
LOS Assert		-26			dBm	
LOS De-Assert				-8	dBm	
LOS Hysteresis		0.5			dB	

Notes:

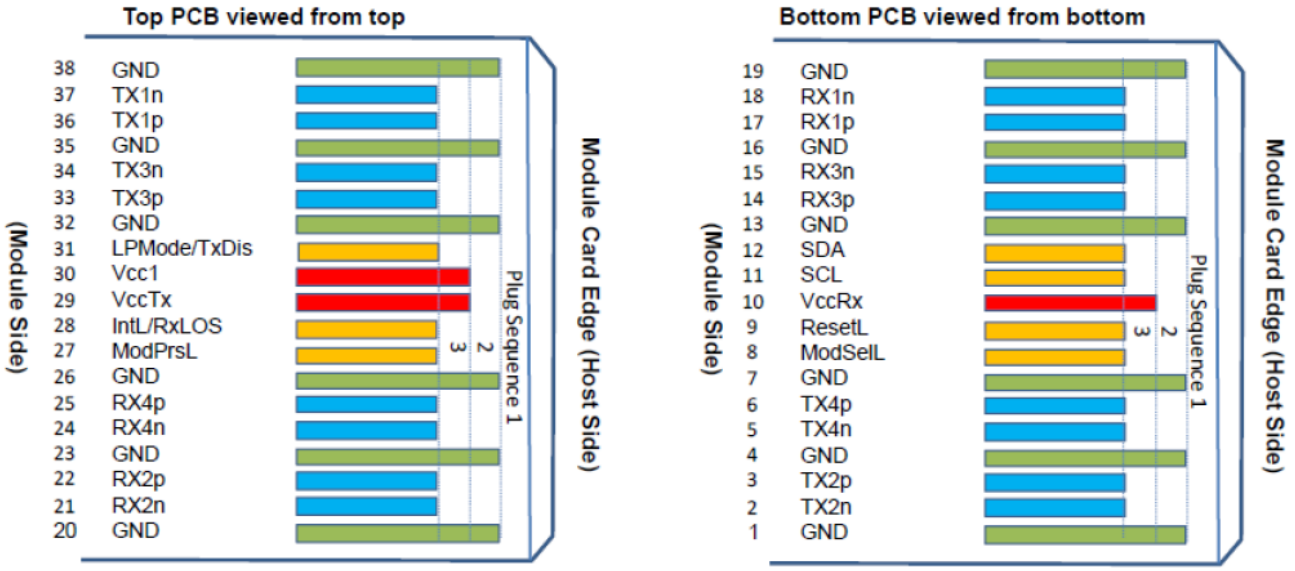
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even If the TDECQ <1.4 dB, the OMAouter (min) has to exceed this value.
3. Transmitter reflectance is defined looking into transmitter.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions

Parameter	Accuracy	Unit
Measured transceiver temperature	±3	°C
Measured transceiver supply voltage	±3	%
Measured Tx bias current	±10	%
Measured Tx output power	±3	dB
Measured Rx received average optical power	±3	dB

Pin Assignment



Pin out of Connector Block on Host Board

PIN	Name	Logic	Description	Plug Sequence	Notes
1	GND		Ground	1	1
2	TX2n	CML-I	Transmitter Inverted Data input	3	
3	TX2p	CML-I	Transmitter Non-Inverted Data input	3	
4	GND		Ground	1	1
5	TX4n	CML-I	Transmitter Inverted Data input	3	
6	TX4p	CML-I	Transmitter Non-Inverted Data input	3	
7	GND		Ground	1	1
8	ModSelL	LVTTL-I	Module Select	3	
9	ResetL	LVTTL-I	Module Reset	3	
10	Vcc Rx		+3.3V Power Supply Receiver	2	2
11	SCL	LVCMOS-I/O	2-wire serial interface clock	3	
12	SDA	LVCMOS-I/O	2-wire serial interface data	3	
13	GND		Ground	1	1
14	RX3p	CML-O	Receiver Non-Inverted Data Output	3	
15	RX3n	CML-O	Receiver Inverted Data Output	3	

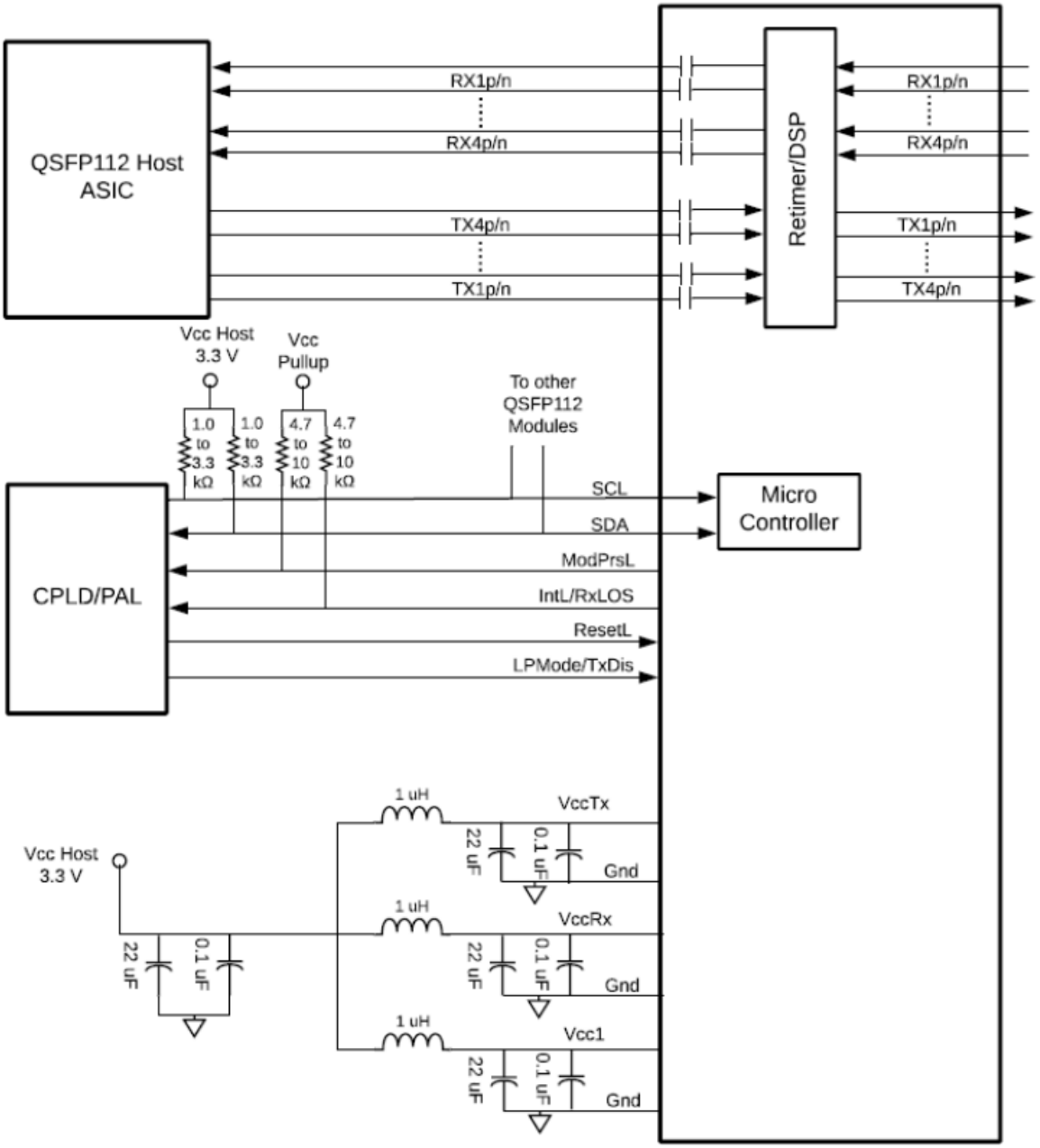
16	GND		Ground	1	1
17	RX1p	CML-O	Receiver Non-Inverted Data Output	3	
18	RX1n	CML-O	Receiver Inverted Data Output	3	
19	GND		Ground	1	1
20	GND		Ground	1	1
21	RX2n	CML-O	Receiver Inverted Data Output	3	
22	RX2p	CML-O	Receiver Non-Inverted Data Output	3	
23	GND		Ground	1	1
24	RX4n	CML-O	Receiver Inverted Data Output	3	
25	RX4p	CML-O	Receiver Non-Inverted Data Output	3	
26	GND		Ground	1	1
27	ModPrsL	LVTTL-O	Module Present	3	
28	IntL/RxLOS	LVTTL-O	Interrupt/optional RxLOS	3	
29	Vcc Tx		+3.3V Power supply transmitter	2	2
30	Vcc1		+3.3V Power supply	2	2
31	LPMode/TxDis	LVTTL-I	Low Power Mode/optional TX Disable	3	
32	GND		Ground	1	1
33	TX3p	CML-I	Transmitter Non-Inverted Data input	3	
34	TX3n	CML-I	Transmitter Inverted Data input	3	
35	GND		Ground	1	1
36	TX1p	CML-I	Transmitter Non-Inverted Data input	3	
37	TX1n	CML-I	Transmitter Inverted Data input	3	
38	GND		Ground	1	1

Notes:

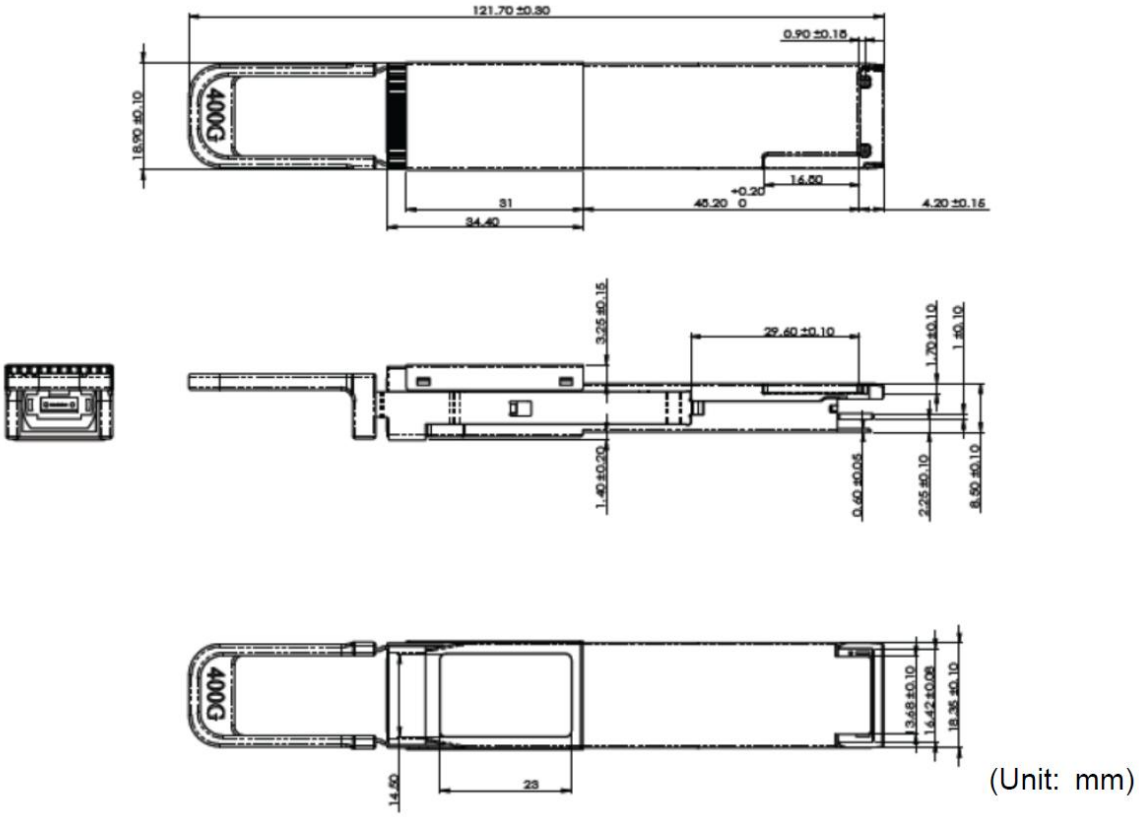
1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are

each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

Recommended Block Diagram



Mechanical Drawing



(Unit: mm)

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-Q112-DR4-C	**QSFP112**	**53.125 GBd (PAM4) per optical lane**	**500 m**	**0 °C to 70 °C**	**400G Ethernet**	**DDM RoHS**

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	29-Jan-2024	New Release	Jason Hou	Wayne Liao	Tom Tang

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