WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

800G OSFP-RHS 2xFR4 Change to 400G OSFP-RHS FR4 Transceiver P/N: WST-OR4-FR4-C

Features:

- Hot-pluggable OSFP form factor
- Power dissipation <11W
- 7nm DSP scheme design and Free space technology
- Maximum link length of 2km on Single Mode Fiber (SMF)
- OSFP RHS form factor
- Duplex LC receptacles
- 3.3V power supply
- I2C management interface
- Operating Case Temperature: 0 to 70°C

Applications:

- Ethernet
- Data Center Interconnect
- 400GBASE-FR4
- Cloud Networks

Standards:

- Compliant with OSFP MSA
- Compliant with IEEE 802.3cK
- Compliant with IEEE 802.3cu
- Compliant with CMIS Rev 5.1
- ROHS-6: Environment Safety

Absolute Maximum Ratings

Absolute maximum ratings are those beyond which damage to the device may occur. Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature Range	T_{STG}	-40	+85	^{0}C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity	RH	10	90	%	Note 1

Note:

1. Non-condensing

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Supply Voltage	T_{CASE}	3.135	3.3	3.465	^{0}C	
Operating Case Temperature	Vcc	0		70	V	
Module Power Dissipation	P_{DISS}			11	W	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		

Link Distance over SMF				2000	M	

Electric Specification for Low Speed Signal

Parameter	Symbol	Min	Max	Units	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus cpacitive load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor,max
			200	pF	1.6k Ohms Pull up resistor,max
V_INT/RSTn_1		0	1	V	for No Module
V_INT/RSTn_2		0	1	V	for Module installed, H_RSTn=Low
V_INT/RSTn_3		1.5	2.25	V	for Module installed, H_RSTn=High,M_INT=Low
V_INT/RSTn_4		2.75	3.465	V	for Module installed, H_RSTn=High,M_INT=High
V_LPWn/PRSn _1		0	1.1	V	for Module installed, H_LPWn=Low
V_LPWn/PRSn _2		1.4	2.25	V	for Module installed, H_LPWn=High
V_LPWn/PRSn _3		2.75	3.465	V	for No Module

Electric Specification for High Speed Signal

Module iutput characteristics at TP1

Parameter	Min	Typical	Max	Unit	Notes
Signaling rate, each lane	53.125±100ppm			GBd	
Differential peak-peak Input Voltage Tolerance	750			mV	
Peak-to-peak AC common-mode voltage					
Low-frequency, VCMLF	32			mV	
Full-band, VCMFB	80				
Differential-mode to common-mode return loss,RLcd	Equation (120G-2)			dB	802.3ck
Effective return loss, ERL	8.5			dB	802.3ck
Differential termination mismatch			10	%	

Module stressed input tolerance		See 120G.3.4.3			802.3ck
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage tolerance	-0.35		2.85	V	

Module output characteristics at TP4

Parameter	Min	Typical	Max	Unit	Notes
Signaling rate, each lane (nominal) 53.125a	53.125±100ppm			GBd	
Peak-to-peak AC common-mode voltage					
Low-frequency, VCMLF			32	mV	
Full-band, VCMFB			80		
Differential peak-to-peak output voltage					
Short mode			600	mV	
Long mode			845		
Eye height	15			mV	
Vertical eye closure, VEC			12	dB	
Common-mode to differential-mode return loss, RLdc	Equation (120G–1)			dB	
Effective return loss, ERL	8.5			dB	
Differential termination mismatch			10	%	
Transition time	8.5			ps	
DC common-mode voltage tolerance (range)	-0.35		2.85	V	

Optical Characteristics

Transmitter Parameter	Lane	Min	Typical	Max	Units
Transmitter					
Lane Wavelength Range	Lane 0	1264.5	1271	1277.5	nm
	Lane 1	1284.5	1291	1297.5	nm
	Lane 2	1304.5	1311	1317.5	nm
	Lane 3	1324.5	1331	1337.5	nm
Average launch Power per lane		-3.2		4.4	dBm
Total Average launch power				10.4	dBm

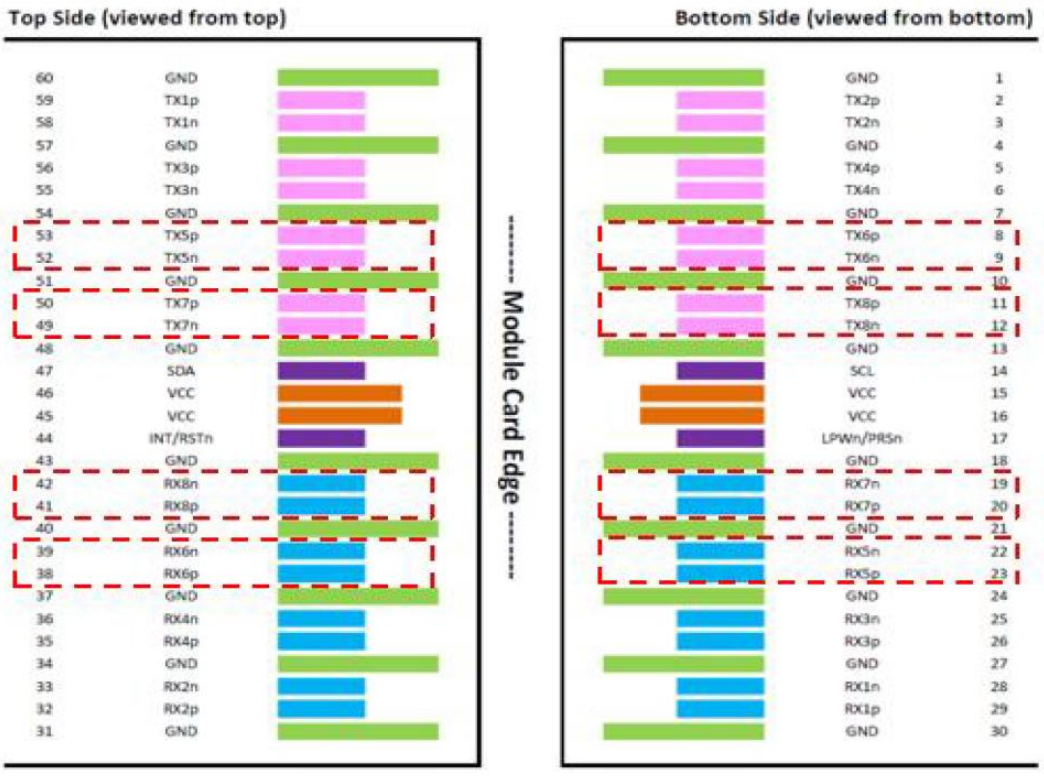
Outer Optical Modulation Amplitude (OMAouter), each lane, for TDECQ <1.4 dB for 1.4 dB ≤TDECQ ≤3.4 dB		0.2 -1.6 +TDECQ		3.7	dBm
Difference in launch power between any two lanes (OMAouter)				3.9	dB
Average Launch Power per Lane @ TX Off State				-16	dBm
Launch Power in OMAouter minus TDECQ, each Lane for ER ≥4.5dB for ER < 4.5dB		-1.7 -1.6			dBm
Transmitter and Dispersion Eye Closure for PAM4, each Lane				3.4	dB
Extinction Ratio		3.5			dB
Relative Intensity Noise (OMA)				-136	dB/Hz
Side-Mode Suppression Ration (SMSR)		30			dB
Optical Return Loss Tolerance				17.1	dB
Transmitter Reflectance				-26	dB
Transmitter Output Power Monitoring Accuracy		-3		3	dB
TDECQ – 10*log10(Ceq), each Lane				3.4	dB
Transmitter transition time				17	ps
Receiver					
Lane Wavelength Range	Lane 0	1264.5	1271	1277.5	nm
	Lane 1	1284.5	1291	1297.5	nm
	Lane 2	1304.5	1311	1317.5	nm
	Lane 3	1324.5	1331	1337.5	nm
Damage Threshold		5.4			dBm
Average Receive Power, each lane		-7.2		4.4	dBm
Receiver Power, each lane (OMA)				3.7	dBm
Receiver Reflectance				-26.0	dB
Difference in receive Power between any Two Lanes(OMAouter)				4.1	dB
Receiver Sensitivity each lane (OMAouter)				max(-4.6,SECQ- 6.0)	dBm
Stressed Receiver Sensitivity (OMAouter), each				-2.6	dBm
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ),Lane under Test			3.4		dB

SECQ – 10*log10(Ceq), lane under test			3.4		dB
OMAouter of each Aggressor Lane			1.5		dBm
RX_LOS_Assert Min/Max		-24			dBm
RX_LOS_De-Assert Min/Max				-13	dBm
RX_LOS_Hysteresis			2.5		dm

Digital Diagnostic Monitoring Specifications

Parameters	Unit	Specification
Temperature Monitor absolute error	° C	± 3
Supply Voltage Monitor absolute error	%	± 5
I_bias Monitor absolute error	%	± 10
Received Power (Rx) Monitor absolute error	dB	± 3.0
Transmit Power (Tx) Monitor absolute error	dB	± 3.0

Pin Assignment

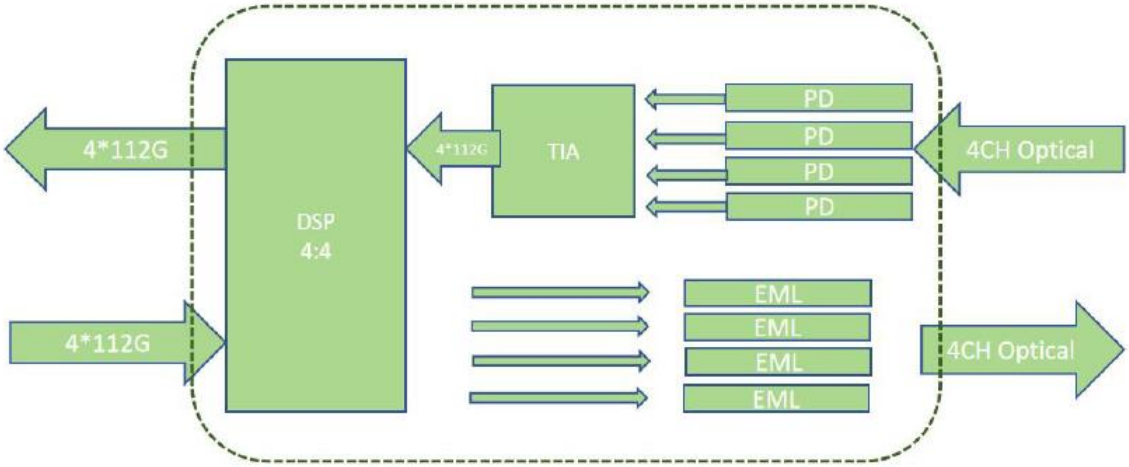


For 400G OSFP FR4 end, Only CH1~CH4 available. CH5~CH8 not connect, TX5~8p/n,RX5~8p/n not connect

Module Signal PIN Descriptions (compliant OSFP MSA Rev 5.0)

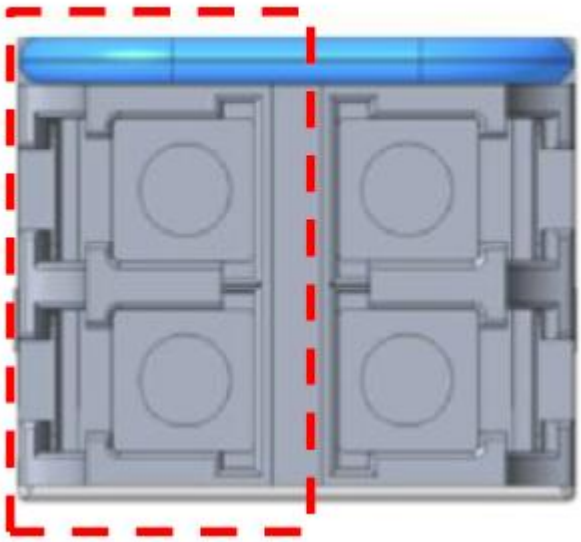
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Block Diagram of Transceiver

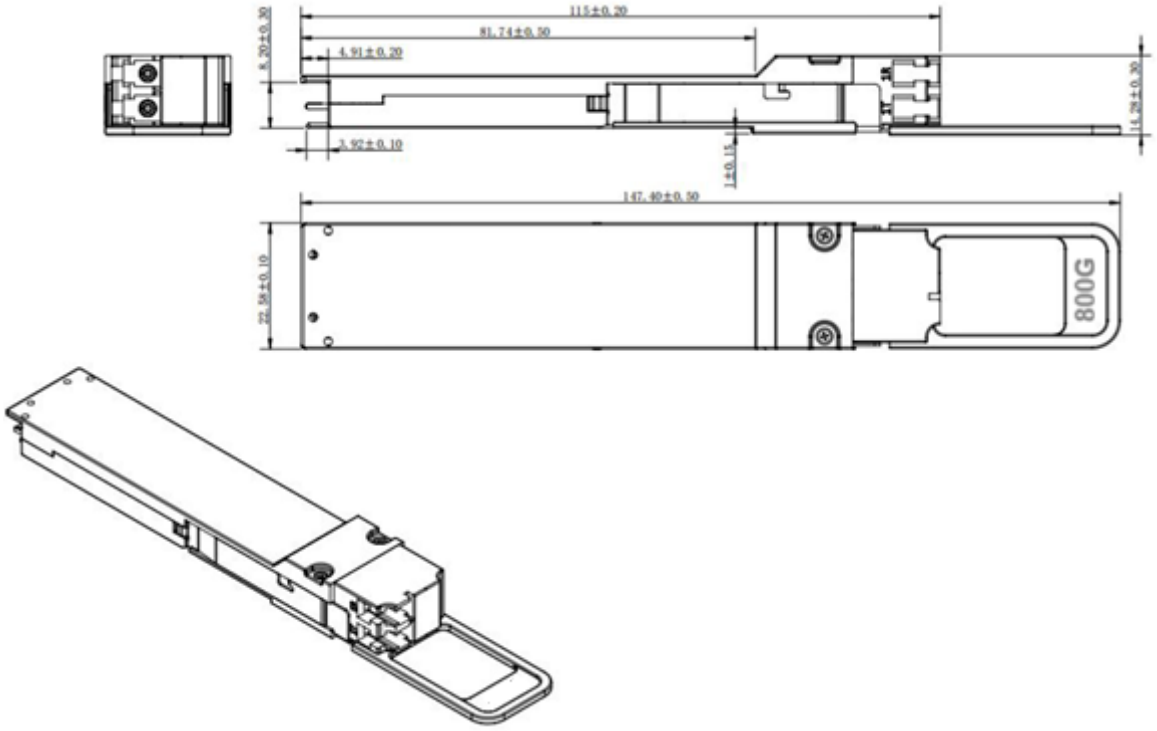


Optical Interface

The Dual Duplex LC module receptacle can use for a 800G OSFP Type For 400G OSFP FR4 end, Just use half.



Mechanical Drawing



Unit: mm

Note: 800G OSFP Housing modified to 400G OSFP RHS, Only the top cover was modified

Ordering Information

Part No	Specification								
	Package	Data rate	Laser	Optical Power	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-OR4-FR4-C	OSFP-RHS	53.125Gbps (PAM4) per channel	1271 nm 1291 nm 1311 nm 1331 nm	-3.2~ +4.4 dBm	max(-4.6,SECQ- 6.0)	0~70°C	2km	DDM RoHS	Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	20-Aug-2025	New Issue	Joanne Ni	Min Liu	Wayne Liao

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