WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

400G QSFP-DD to OSFP112-RHS Active Optical Cable
P/N: WS-D4R4-AOCxCyyS

Standard:

- IEEE 802.3 (400GAUI-4 and 400GAUI-8)
- IEEE 802.3bs 400GBASE-DR4
- OSFP MSA
- QSFP-DD MSA
- CMIS Rev. 4.0 or later

Applications:

- 400G Ethernet data center interconnects
- OSFP112-RHS to QSFP-DD interconnect links
- High-density switch and router connections
- Cloud and hyperscale data center networking

Features:

- Supports 400 Gb/s aggregate data rate (4 × 106.25 Gb/s PAM4)
- OSFP compliant with OSFP MSA (RHS form factor)
- QSFP-DD compliant with QSFP-DD MSA
- Electrical interface: 400GAUI-4 (OSFP112 side) and 400GAUI-8 (QSFP-DD side)
- Optical interface compliant with 400GBASE-DR4
- 4 parallel optical lanes over single-mode fiber (SMF), up to 500 m
- Power consumption:
  Max. 9 W (OSFP end)
  Max. 10 W (QSFP-DD end)
- Single 3.3 V power supply
- Operating case temperature: 0 °C to 70 °C
- RoHS compliant

Description

The 400G QSFP-DD to OSFP112-RHS Active Optical Cable (AOC) is designed for high-speed data center interconnect applications. It supports an aggregate data rate of 400 Gb/s using 4 lanes of 106.25 Gb/s PAM4 signaling over single-mode fiber. The cable provides a direct connection between QSFP-DD and OSFP112-RHS interfaces, compliant with IEEE 802.3 400GAUI and 400GBASE-DR4 specifications, enabling reliable transmission up to 500 m over SMF.

The product integrates optical engines and electrical interfaces within cable assemblies to deliver low power consumption, high reliability, and simplified system integration for short to medium-reach interconnects.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes.
Maximum Supply Voltage	V_{cc}	-0.3		3.6	V	
Storage Temperature	T_{sto}	-40		85	℃	
Relative Humidity	RH	5		85	%	Non-condensing

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes.
Operating Case Temperature	TC	0		+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation per QSFP-DD	Pd			10	W	1
Power Dissipation per OSFP112-RHS	Pd			9	W	1
Supply Current per QSFP-DD	Icc			3.2	A	1
Supply Current per OSFP112-RHS	Icc			2.9	A	1
Bit Rate per lane	BR		53.125		GBd	PAM4

Note:
1 Per terminal

Electrical Specification High Speed Signal

Parameter	Symbol / Test Point	Min.	Typ.	Max.	Unit.	Notes
Pre-FEC BER	BER_{pre}			1E-6		
Post-FEC BER	BER_{pos}			1E-12		KP4
Signaling Rate per Lane	SRL		53.125		GBd	

QSFP-DD Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	

Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

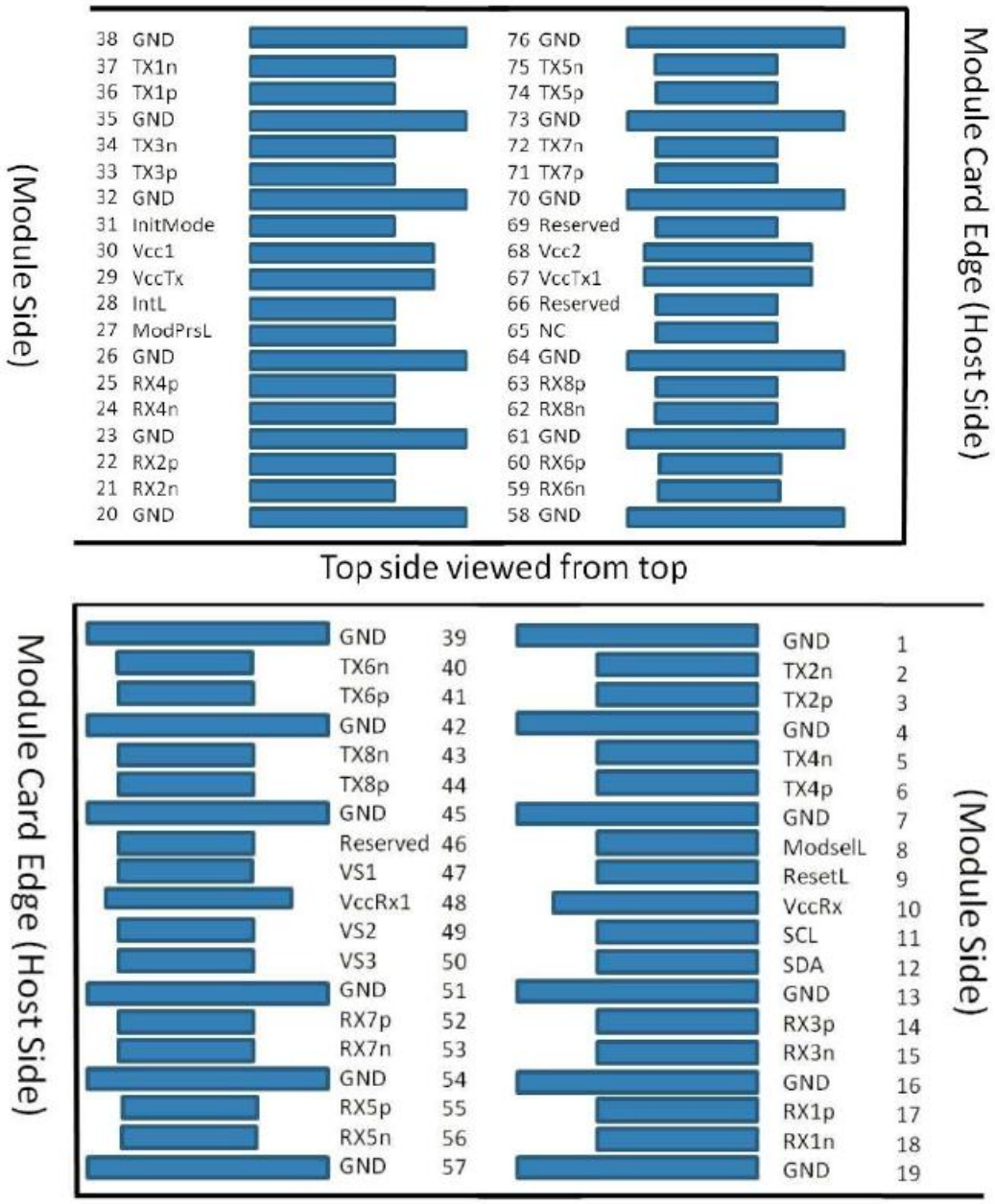
Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage

OSFP112-RHS Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Signaling rate, each lane (range)		52.125 ± 100 ppm			GBd	
Transmitter (each Lane)						
Differential pk-pk voltage tolerance (min)	TP1a	750			mV	
Peak-to-peak AC common-mode voltage tolerance (min)	TP1a				mV	
Low-frequency, VCMLF			32			
Full-band, VCMFB			80			
Differential Termination Mismatch	TP1			10	%	
Module stressed input tolerance	TP1a	See IEEE P802.3ck™/D3.0 120G.3.4.3				
Single-ended voltage tolerance	TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance	TP1	-0.35		2.85	V	
Receiver (each Lane)						
Peak-to-peak AC common-mode voltage (max)	TP4				mV	
Low-frequency, VCMLF			32			
Full-band, VCMFB			80			
Differential peak-to-peak output voltage (max)	TP4					
Short mode			600		mV	
Long mode			845			
Eye height	TP4	15			mV	
Vertical eye closure, VEC	TP4			12	dB	
Differential Termination Mismatch	TP4			10	%	
Transition time	TP4	8.5			ps	
DC common-mode voltage tolerance	TP4	-0.35		2.85	V	

Pin Descriptions of QSFP-DD



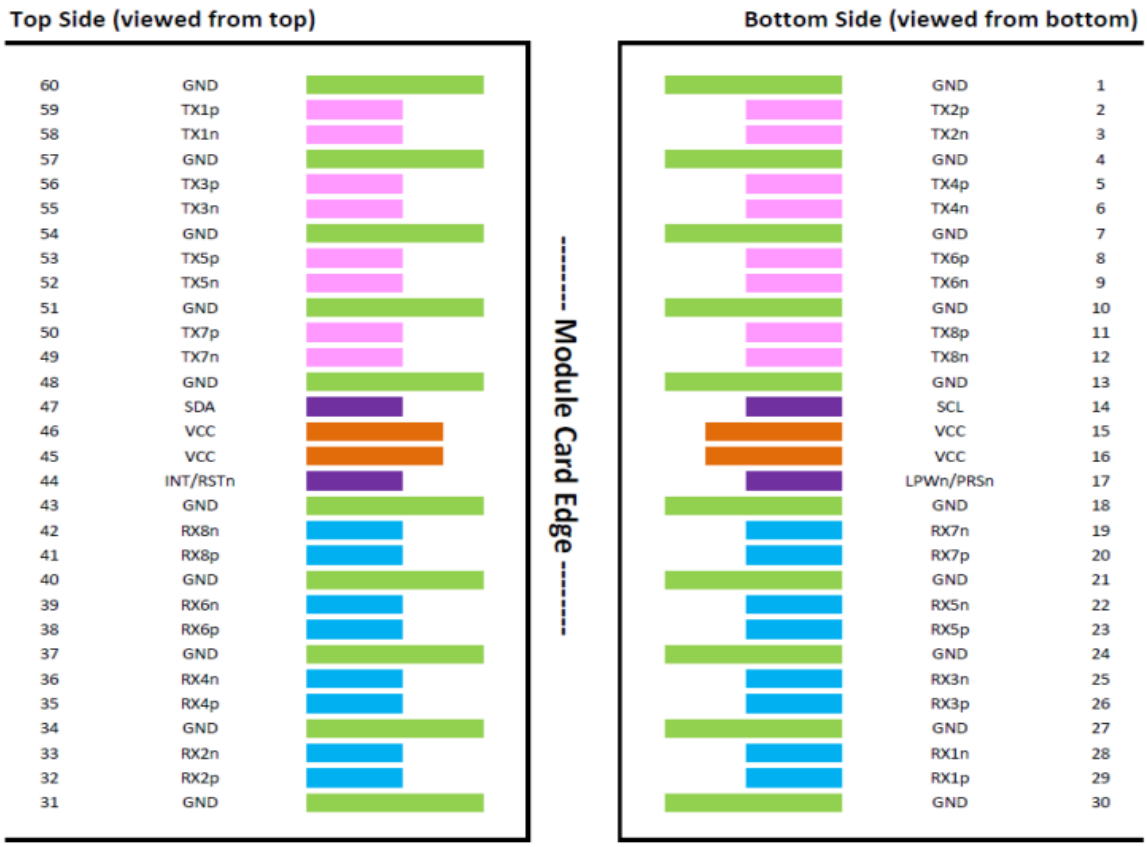
Pin out of Connector Block on Host Board

PIN	Logic	Symbol	Description	Notes
1		GND	Ground	
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	
8	LVTTL-I	ModselL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	
20		GND	Ground	
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt.	
29		Vcc Tx	+3.3V Power supply transmitter	
30		Vcc1	+3.3V Power supply	
31	LVTTL-I	InitMode	Initialization mode	

32		GND	Ground	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	
39		GND	Ground	
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-inverted Data Input	
42		GND	Ground	
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-inverted Data Input	
45		GND	Ground	
46		Reserved		
47		VS1	Module Vendor Specific 1	
48		VccRx1	3.3V Power Supply	
49		VS2	Module Vendor Specific 2	
50		VS3	Module Vendor Specific 3	
51		GND	Ground	
52	CML-O	Rx7p	Receiver Non-inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	
55	CML-O	Rx5p	Receiver Non-inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	
58		GND	Ground	
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-inverted Data Output	
61		GND	Ground	
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-inverted Data Output	
64		GND	Ground	

65		NC	Not connected	
66		Reserved		
67		VccTx1	3.3V Power Supply	
68		Vcc2	3.3V Power Supply	
69		Reserved		
70		GND	Ground	
71	CML-I	Tx7p	Transmitter Non-inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	
74	CML-I	Tx5p	Transmitter Non-inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	

Pin Assignment of OSFP112-RHS



Pin out of Connector Block on Host Board

Pin Description

Name	Direction	DESCRIPTION
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host.
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module.

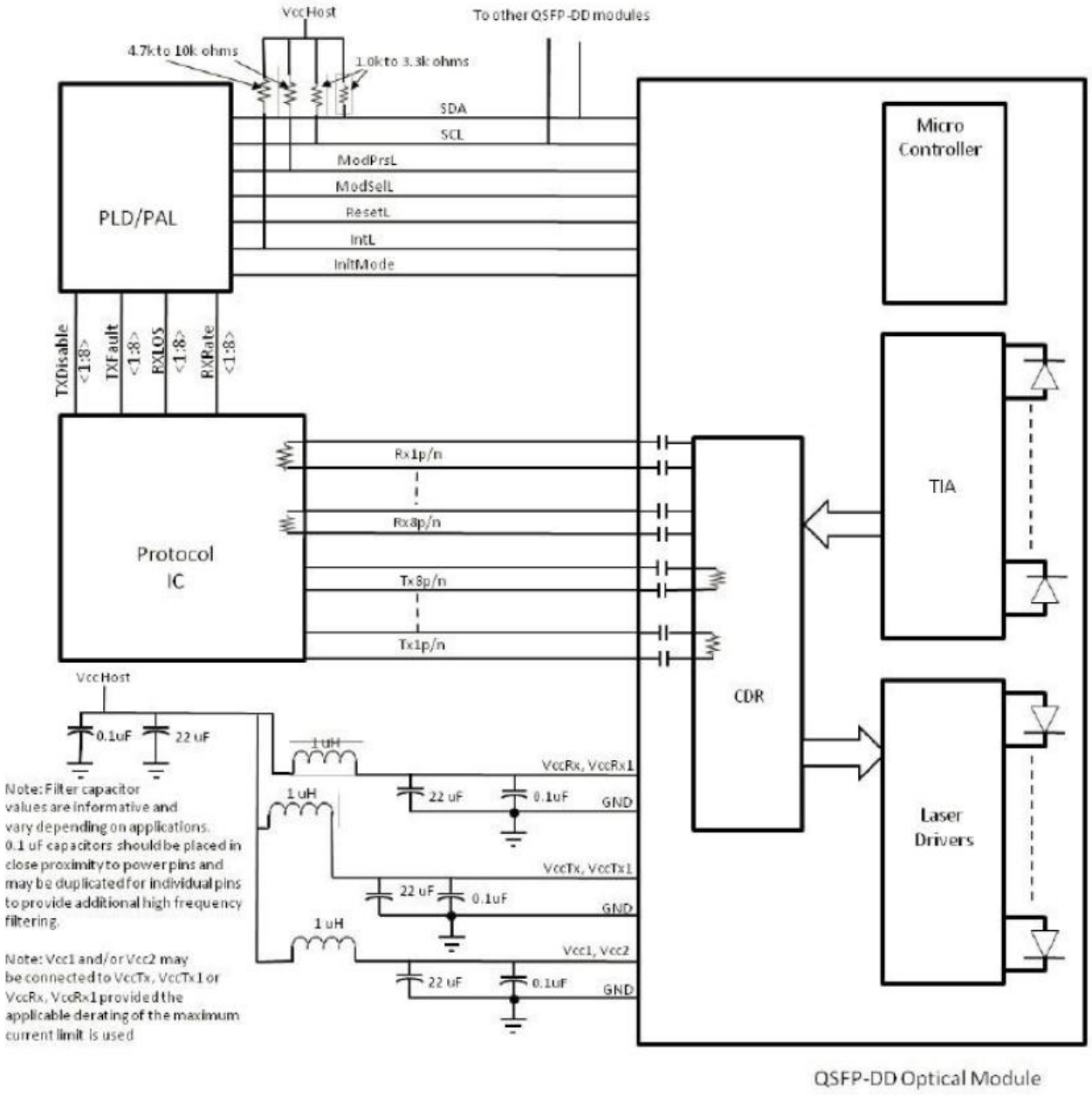
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

Pin List

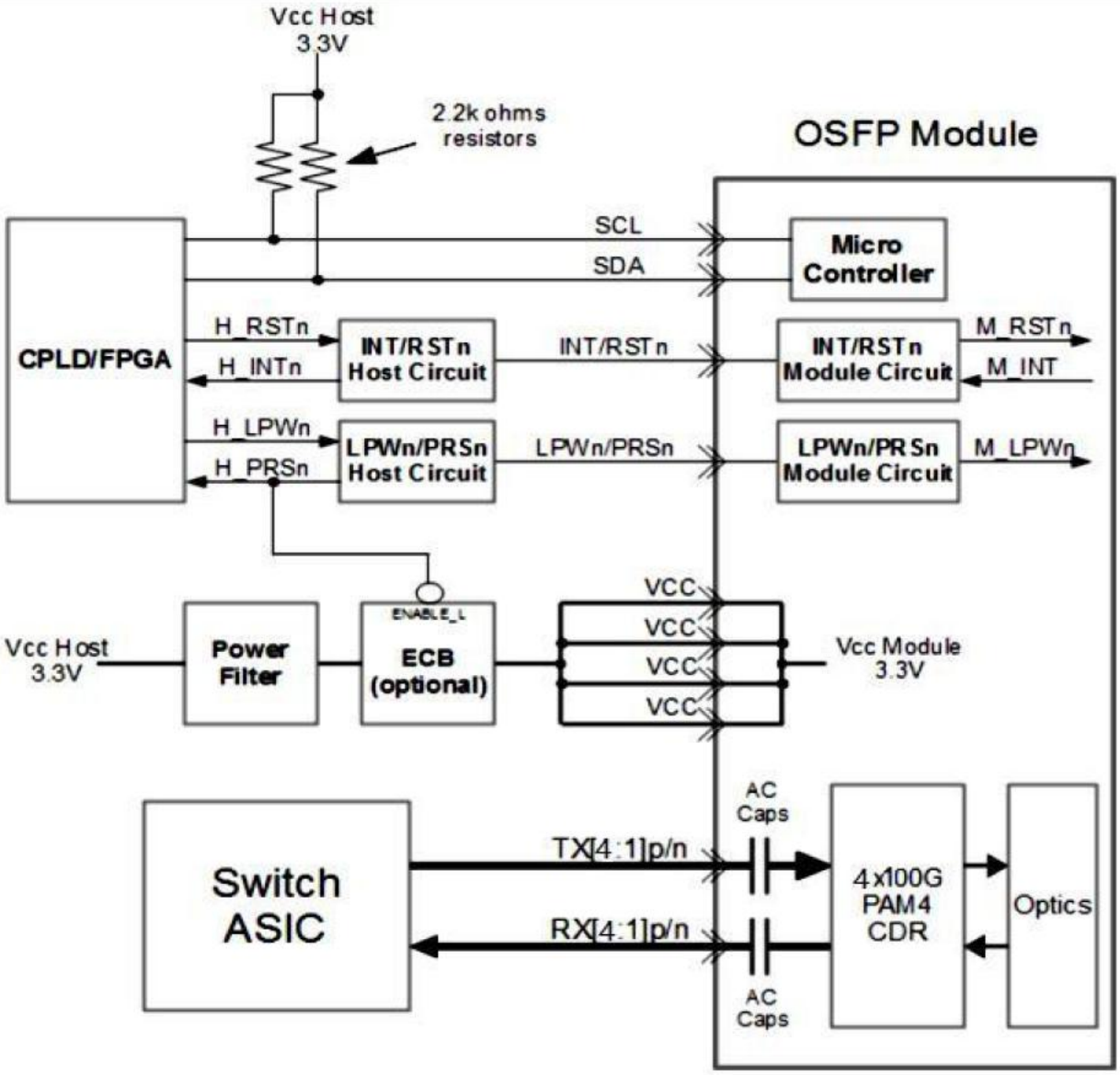
PIN	Logic	Symbol	DESCRIPTION	NOTE
1		GND	Ground	
2	CML-I	Tx2p	Transmitter Data Non-Inverted	
3	CML-I	Tx2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	Tx4p	Transmitter Data Non-Inverted	
6	CML-I	Tx4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	Tx6p	Transmitter Data Non-Inverted	Unused in 400G Mode
9	CML-I	Tx6n	Transmitter Data Inverted	Unused in 400G Mode
10		GND	Ground	
11	CML-I	Tx8p	Transmitter Data Non-Inverted	Unused in 400G Mode
12	CML-I	Tx8n	Transmitter Data Inverted	Unused in 400G Mode
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	Open-Drain with pull up resistor on Host
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	See pin description
18		GND	Ground	
19	CML-O	Rx7n	Receiver Data Inverted	Unused in 400G Mode
20	CML-O	Rx7p	Receiver Data Non-Inverted	Unused in 400G Mode
21		GND	Ground	
22	CML-O	Rx5n	Receiver Data Inverted	Unused in 400G Mode

23	CML-O	Rx5p	Receiver Data Non-Inverted	Unused in 400G Mode
24		GND	Ground	
25	CML-O	Rx3n	Receiver Data Inverted	
26	CML-O	Rx3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	Rx1n	Receiver Data Inverted	
29	CML-O	Rx1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	Rx2p	Receiver Data Non-Inverted	
33	CML-O	Rx2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	Rx4p	Receiver Data Non-Inverted	
36	CML-O	Rx4n	Receiver Data Inverted	

Transceiver Module Block Diagram

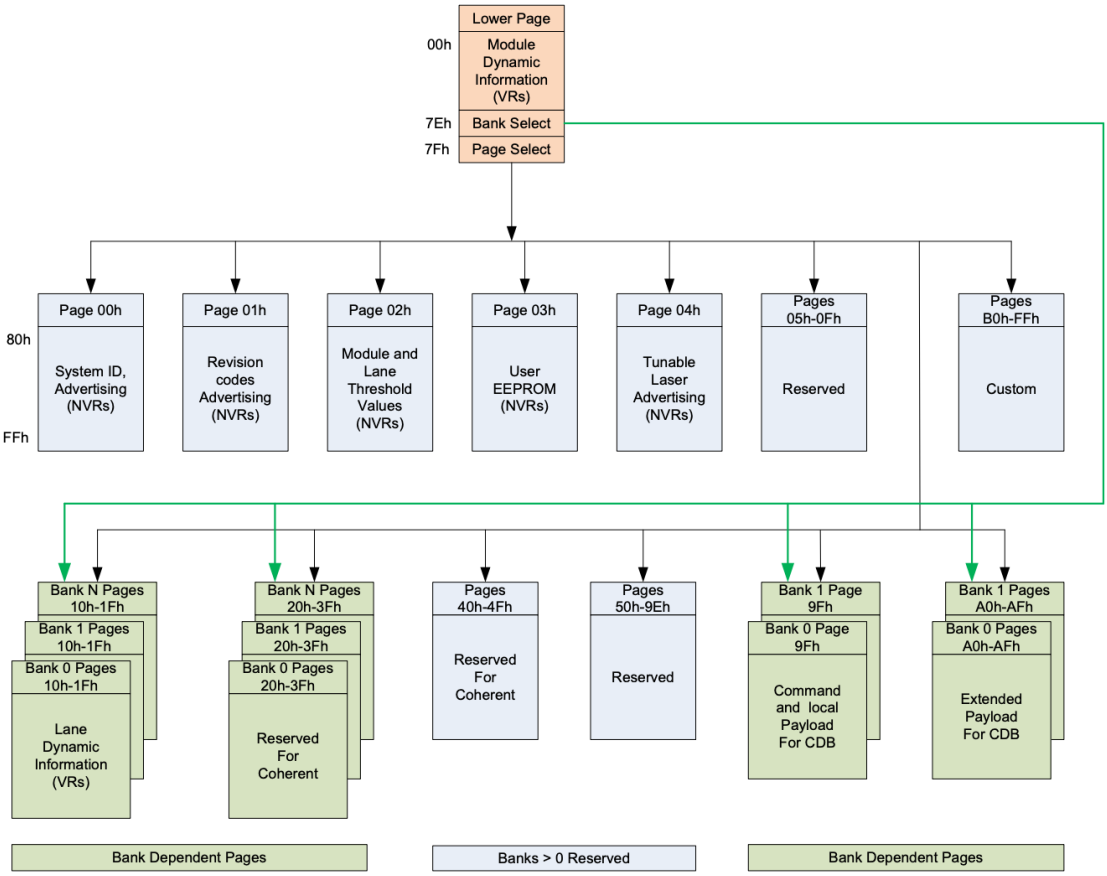


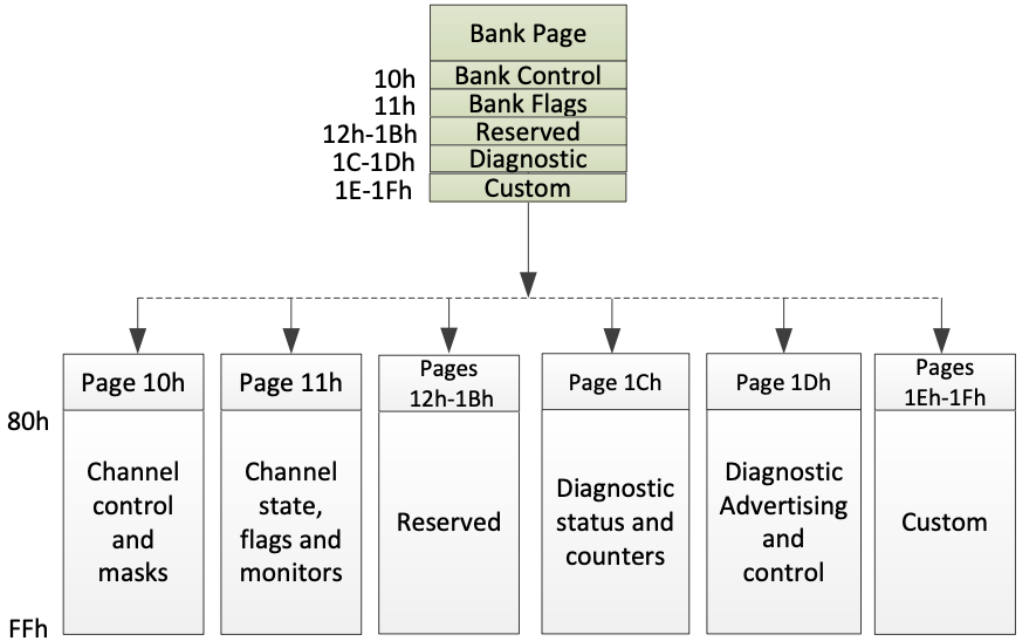
QSFP-DD SIDE



OSFP112 SIDE

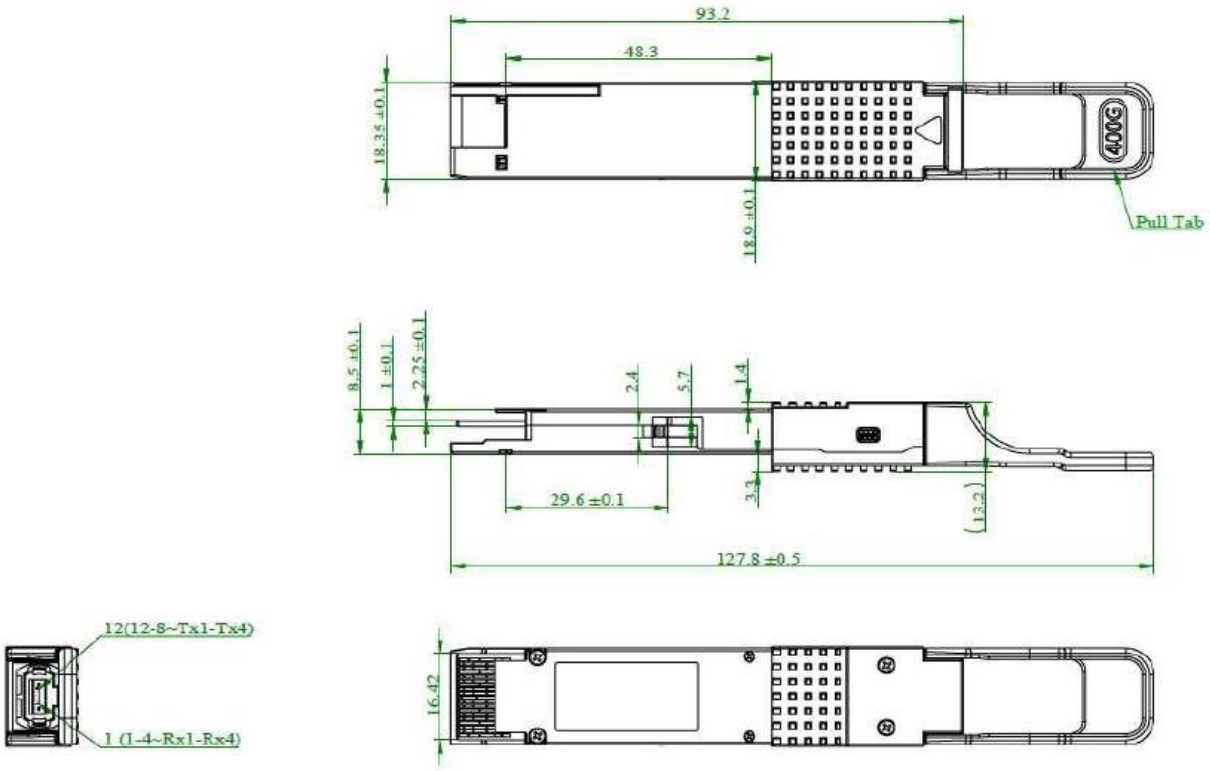
Memory Map (Compliant with CMIS Rev4.0)





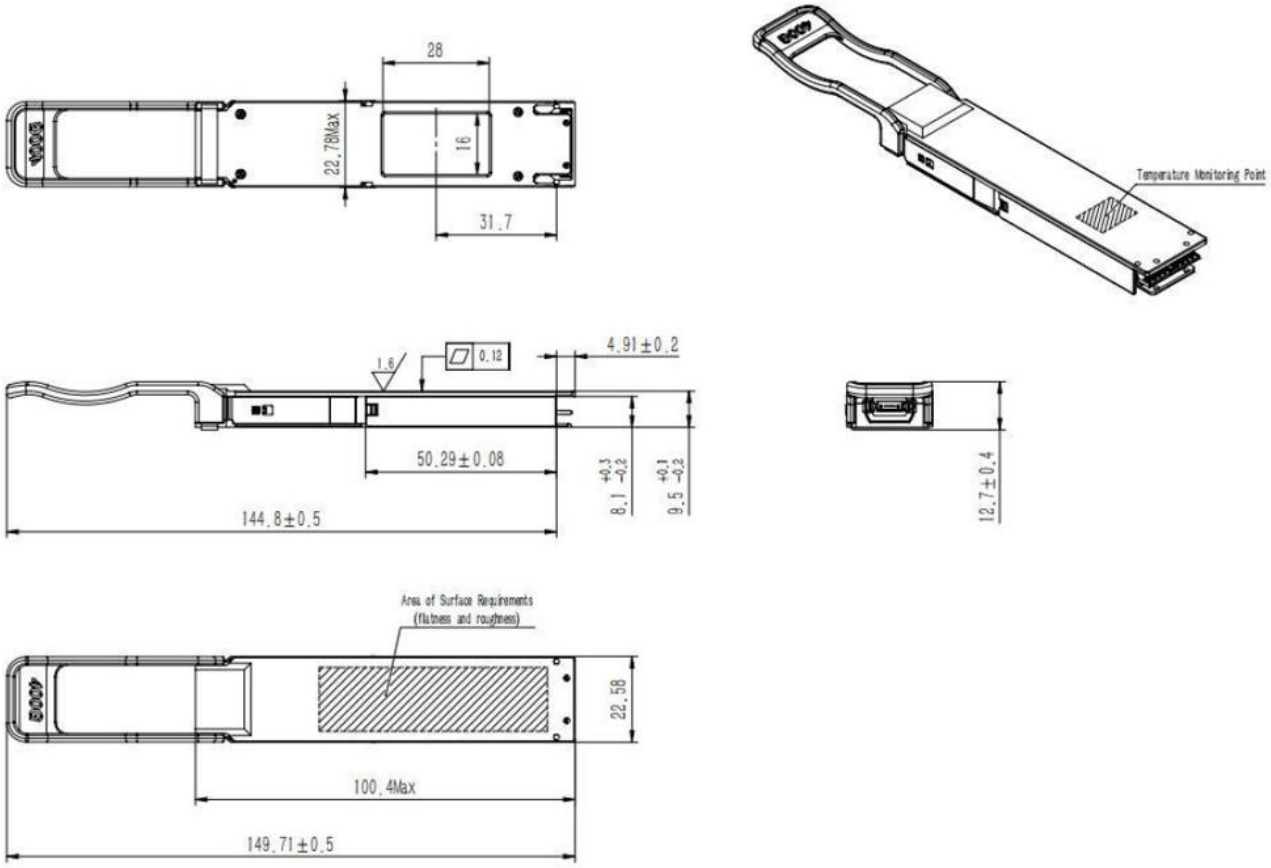
Mechanical Drawing

a. QSFP-DD



Unit: mm

b. OSFP112



Unit: mm

Cable Length

Cable Length (Unit: m)	Tolerant (Unit: cm)
＜ 1.0	+5 / -0
1.0 ~ 4.5	+15 / -0
5.0 ~ 14.5	+30 / -0
≥ 15.0	+2% / -0

Cable Diameter: 3.0 mm

Minimum bending radius: 30 mm

Ordering Information

Part No	Specification							
	Package	Data rate	Laser	Fiber	Cable Type	Cable Length	Temp.	Application
WS-D4R4-AOCLC01S	QSFP-DD to OSFP112-RHS	400 Gb/s	1310 nm	SMF	Round LSZH	1 m	0 ~ 70 °C	400GbE Interconnect
WS-D4R4-AOCLC03S	QSFP-DD to OSFP112-RHS	400 Gb/s	1310 nm	SMF	Round LSZH	3 m	0 ~ 70 °C	400GbE Interconnect
WS-D4R4-AOCLC05S	QSFP-DD to OSFP112-RHS	400 Gb/s	1310 nm	SMF	Round LSZH	5 m	0 ~ 70 °C	400GbE Interconnect
WS-D4R4-AOCLC10S	QSFP-DD to OSFP112-RHS	400 Gb/s	1310 nm	SMF	Round LSZH	10 m	0 ~ 70 °C	400GbE Interconnect
WS-D4R4-AOCLC15S	QSFP-DD to OSFP112-RHS	400 Gb/s	1310 nm	SMF	Round LSZH	15 m	0 ~ 70 °C	400GbE Interconnect
WS-D4R4-AOCxCyyS	QSFP-DD to OSFP112-RHS	400 Gb/s	1310 nm	SMF	Round LSZH, Round OFNP, Round OFNR	yy m	0 ~ 70 °C	400GbE Interconnect

Note:

Cable jacket type: x= L for LSZH, P for OFNP, and R for OFNR, X for any of the above (OFNR, OFNP, or LSZH)

Length: yy meters

Cable length and type options are available upon request. Please contact our sales for detailed information

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	19-Feb-2025	New Issue	Jason Hou	Wayne Liao	Tom Tang

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