Data Sheet

400G QSFP-DD Active Optical Cable (AOC)
P/N: WS-QD4-AOC8LCxx4

Features:

- 400 Gb/s aggregate data rate
- 8 electrical lanes at 53.125 Gb/s PAM4
- Maximum length of 70m with FEC
- Hot pluggable
- Single 3.3 V power supply
- Power dissipation < 8W per end (with CDR)
- Digital diagnostic monitoring support
- Operating case temperature: 0 °C to +70 °C
- RoHS compliant

Applications:

- 400G interconnects over multimode fiber
- Datacom and telecom switching and routing applications

Standards:

- IEEE 802.3bs compliant
- QSFP-DD MSA compliant
- CMIS 4.0 management interface compliant

Description

The WS-QD4-AOC8LCxx4 module is a 400G QSFP-DD to QSFP-DD Active Optical Cable (AOC) designed for short-range data communication and interconnect applications. It provides eight electrical lanes operating with a PAM4 modulation scheme at 53.125 Gb/s for each lane, supporting a maximum OM4 multimode fiber (MMF) length of up to 70m with FEC. The cable integrates optical and electrical components within a QSFP-DD form factor on both ends, utilizing an integrated pre-terminated fiber. Designed with an internal Retimer/DSP and operating on a single 3.3V power supply, it features a power dissipation of < 8W per end (with CDR), making it optimized for 400G interconnection in datacom/telecom switch and router connections.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-10	70	°C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity	RH	5	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical Signal Rate (per lane)		53.125 ± 100 ppm			Gb/s	PAM4
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T_C	0		70	°C	
Power Consumption (each end)	P_C			8	W	

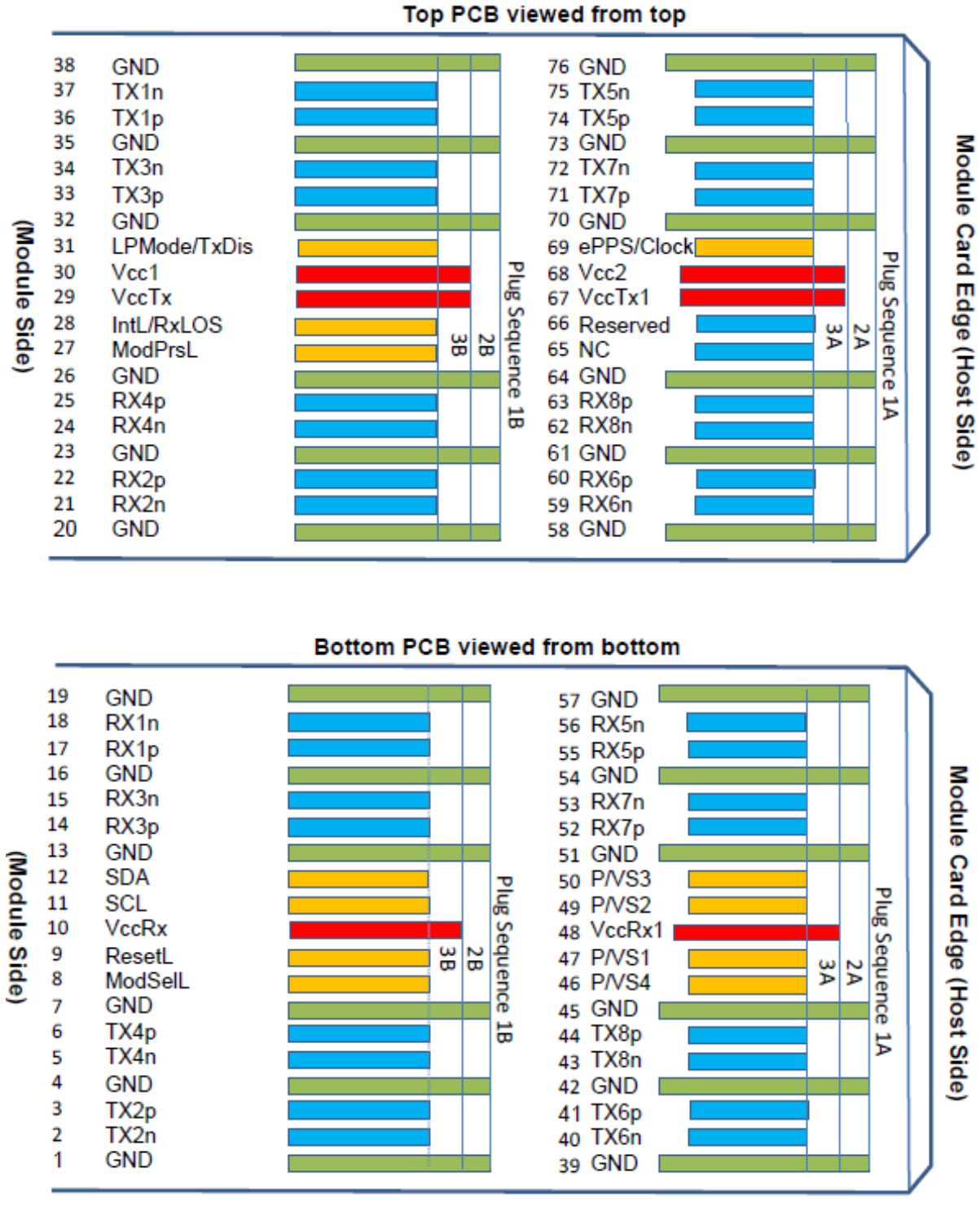
Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Test Point	Min	Typ	Max	Unit	Note
High Speed Electrical Input Characteristics						
Signaling speed (per lane)	TP1	53.125 ± 100 ppm			Gb/s	
Differential pk-pk input voltage tolerance	TP1a	900			mV	
Differential termination mismatch	TP1a			10	%	
Single-ended voltage tolerance	TP1a	-0.4		3.3	V	
DC common-mode voltage	TP1	-0.35		2.85	V	
High Speed Electrical Output Characteristics						
Signaling speed (per lane)	TP4	53.125 ± 100 ppm			Gb/s	
Differential peak-to-peak output voltage	TP4			0.9	V	
Near-end ESMW (Eye symmetry mask width)	TP4	0.265			UI	
Near-end Eye height, differential	TP4	0.07			V	
DC common mode voltage	TP4	-0.35		2.85	V	
Transition time (20% to 80%)	TP4	9.5			ps	

Digital Diagnostic Monitor Accuracy (Under Recommended Operating Conditions)

Parameter	Accuracy	Unit	Note
Measured transceiver temperature	±3	°C	
Measured transceiver supply voltage	±3	%	
Measured Tx bias current	±10	%	

Pin Assignment



Pin out of Connector Block on Host Board

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VCC Rx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VCC Tx	+3.3 V Power Supply Transmitter	2B	2
30		VCC1	+3.3 V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1	1

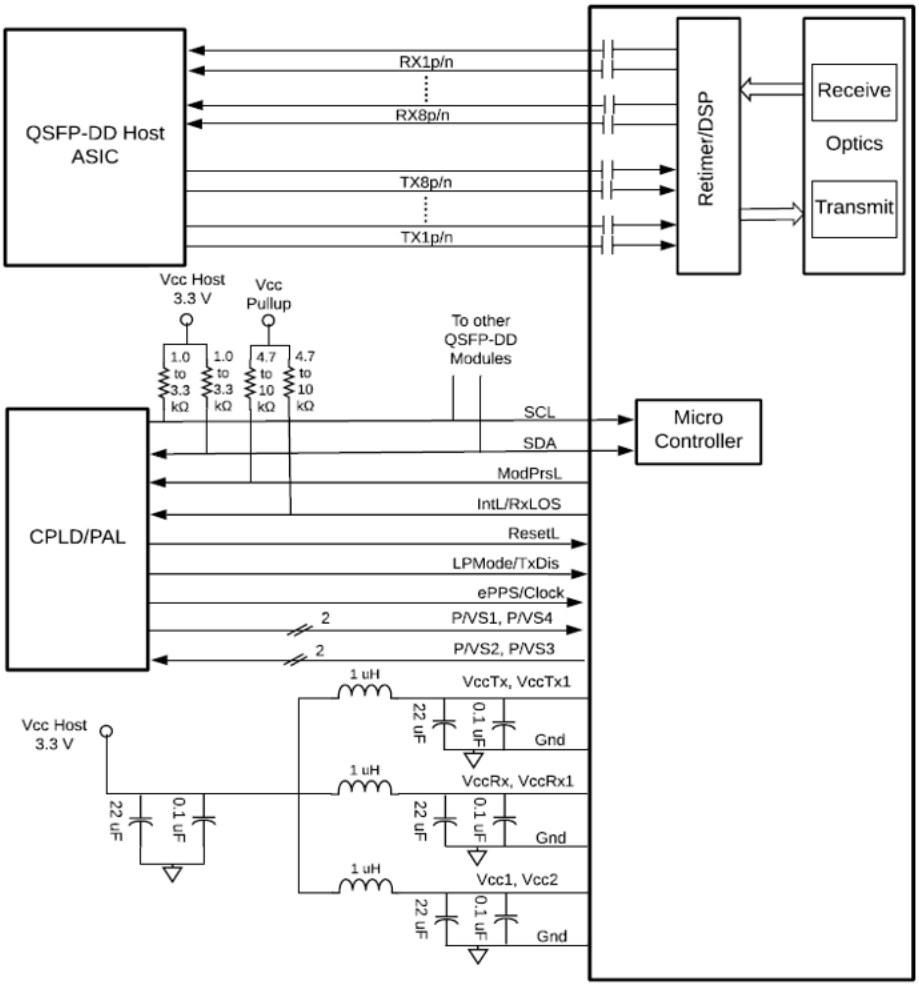
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1B	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VCC Tx1	+3.3 V Power Supply Transmitter	2A	2
68		VCC2	+3.3 V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input (N/C within module)	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	

72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

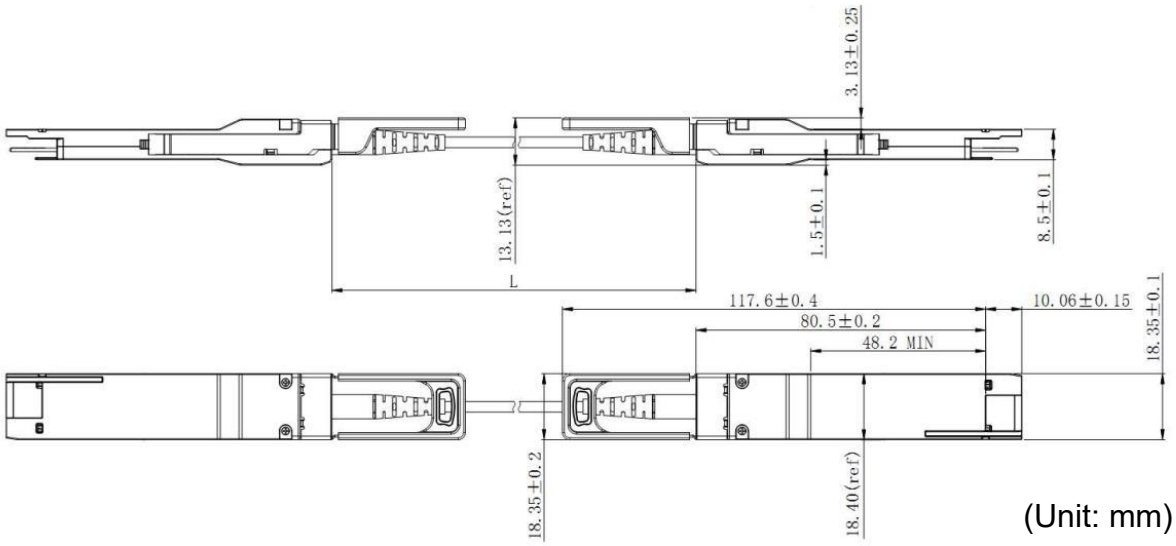
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed above. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Recommended block diagram with host board's connections



Package Dimensions



(Unit: mm)

Cable Length (Unit: m)	Tolerance
1.0 ~ 4.5	±5 cm
5.0 ~ 14.5	±15 cm
15.0 ~ 70	±1.5%

Ordering Information

Part No	Package	Data rate	Laser	Fiber	Cable Type	Cable Length	Temp	Application
WS-QD4-AOC8LC014	QSFP-DD	400 Gb/s	850nm	OM4	LSZH	1m	0~70°C	400G Switch & Router interconnection
WS-QD4-AOC8LC034	QSFP-DD	400 Gb/s	850nm	OM4	LSZH	3m	0~70°C	400G Switch & Router interconnection
WS-QD4-AOC8LC054	QSFP-DD	400 Gb/s	850nm	OM4	LSZH	5m	0~70°C	400G Switch & Router interconnection
WS-QD4-AOC8LC104	QSFP-DD	400 Gb/s	850nm	OM4	LSZH	10m	0~70°C	400G Switch & Router interconnection
WS-QD4-AOC8LC304	QSFP-DD	400 Gb/s	850nm	OM4	LSZH	30m	0~70°C	400G Switch & Router interconnection

Note:

Optional cable type (e.g., OFNR, OFNP), fiber type, and cable lengths may be available upon customer request. Please contact sales for availability.

Modification History

Revision	Date	Description	Originator	Review	Approve
V1.0	8-Sep-2024	New Issue	Henry Chung	Wayne Liao	Tom Tang

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