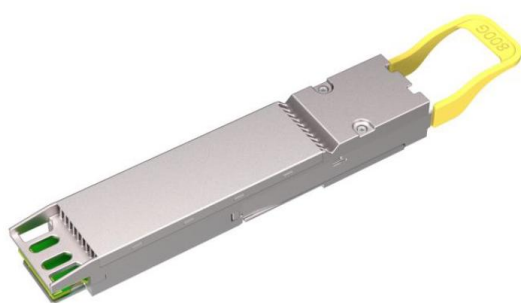


Data Sheet

800G OSFP-RHS 2xDR4 Transceiver Module P/N: WST-OR8-DR4X2-C



Features:

- 800G OSFP-RHS 2xDR4 optical transceiver module
- Supports aggregate data rate up to 800 Gb/s
- 8 optical and electrical lanes at 106.25 Gb/s PAM4
- 8 transmit and 8 receive optical lanes
- Dual MPO-12 optical connectors
- 2xDR4 optical interface over single-mode fiber with maximum link length up to 500 m
- 800GAUI-8 retimed electrical interface
- Digital diagnostic monitoring support
- I2C management interface
- 5 nm DSP design with silicon photonics technology
- Single 3.3 V power supply
- Power consumption: Max. 14.5 W
- Operating case temperature: 0 °C to +70 °C
- RoHS compliant

Applications:

- 800 Gigabit Ethernet links over single-mode fiber
- Supports 2 × 400 G, 4 × 200 G, and 8 × 100 G split modes for breakout applications
- Data center interconnect
- Switch-to-switch and switch-to-router interconnections

Standards:

- Aligned with IEEE 802.3bs 400GBASE-DR4 optical specifications (2 × DR4)
- Aligned with IEEE 802.3ck 100 Gb/s per-lane electrical specifications
- OSFP MSA compliant
- CMIS Rev. 5.1 Management Interface

Description

The WST-OR8-DR4X2-C is an 800G OSFP-RHS 2xDR4 optical transceiver module designed for high-speed data communication and data center interconnect applications over single-mode fiber. It supports an aggregate data rate of 800 Gb/s and transmission distance from 2 m to 500 m over G.652 SMF. The module uses silicon photonics technology and provides a 2xDR4 optical interface through dual MPO-12 connectors in a hot-pluggable OSFP-RHS form factor.

Functional Description

The module provides eight electrical lanes and eight optical lanes operating at 106.25 Gb/s PAM4 per lane. On the transmit side, it converts 8×100 Gb/s PAM4 electrical input signals into 8 parallel optical output signals. On the receive side, it converts 8 parallel optical input signals into 8×100 Gb/s PAM4 electrical output signals. The module supports an 8x100G PAM4 retimed 800GAUI-8 electrical interface and provides standard OSFP management through the I2C/CMIS Rev. 5.1 interface for module configuration, status monitoring, and fault reporting. It operates from a single +3.3 V power supply with a maximum power consumption of 14.5 W and supports commercial case temperature operation from 0 °C to 70 °C.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T _S	-40	85	°C	
Supply Voltage	V _{CC}	-0.5	3.6	V	
Relative Humidity	RH	10	90	%	Non-condensing
Receiver Damage Threshold (per lane)	R _D		+5	dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Optical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T _C	0		70	°C	
Power Consumption	P _{DISS}			14.5	W	
Supply Current	I _{CC}			4625	mA	Calculated from maximum power consumption.
Link Distance (G.652)	DI	2		500	m	
Pre-FEC Bit Error Ratio				2.4×10^{-4}		

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
High Speed Electrical Input Characteristics						
Signaling rate per lane (PAM4 Encoded)	TP1	-100 ppm	53.125	+100 ppm	GBd	
Differential peak-to-peak input voltage tolerance	TP1a	750			mV	
Peak-to-peak AC common-mode voltage						
Low-frequency, VCMLF		32			mV	
Full-band, VCMFB		80			mV	
Differential-mode to common-mode return loss, RLcd		Equation (120G-2)			dB	802.3ck
Effective return loss, ERL		8.5			dB	802.3ck
Differential termination mismatch				10	%	
Module stressed input tolerance			See 120G.3.4.3			802.3ck
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance	TP1	-0.35		2.85	V	
High Speed Electrical Output Characteristics						
Signaling rate per lane (PAM4 Encoded)	TP4	-100 ppm	53.125	+100 ppm	GBd	
Peak-to-peak AC common-mode voltage						
Low-frequency, VCMLF				32	mV	
Full-band, VCMFB				80	mV	
Differential peak-to-peak output voltage						
Short mode				600	mV	
Long mode				845	mV	
Eye height		15			mV	
Vertical eye closure, VEC				12	dB	
Common-mode to differential-mode return loss, RLdc		Equation (120G-1)			dB	
Effective return loss, ERL		8.5			dB	
Differential termination mismatch				10	%	
Transition time		8.5			ps	
DC common-mode voltage tolerance (range)		-0.35		2.85	V	

Optical Characteristics (Under Recommended Operating Conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Signaling speed (per lane)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	λ	1304.5	1310	1317.5	nm	
Average optical power (per lane)	P	-2.9		4	dBm	
OMAouter (per lane)	P _{OMA}	-0.8		4.2	dBm	
Launch power in OMAouter minus TDECQ (per lane)		-2.2			dB	
Transmitter and dispersion eye closure for PAM4 (TDECQ) (per lane)				3.4	dB	
Side mode suppression ratio (SMSR)		30			dB	
Extinction ratio	ER	3.5			dB	
Average launch power of OFF transmitter (per lane)	P _{off}			-15	dBm	
RIN _{21.4OMA}	RIN			-136	dB/Hz	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26	dB	
Receiver						
Signaling speed (per lane)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	λ	1304.5	1310	1317.5	nm	
Average receive power (per lane)		-5.9		4	dBm	
Receive power (OMAouter) (per lane)	R _{OMA}			4.2	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter) (per lane)	RS _{OMA}			-4.4	dBm	1
Stressed receiver sensitivity (OMAouter) (per lane)	SRS _{OMA}			-1.9	dBm	
Stressed receiver sensitivity Test Conditions						
Stressed eye closure for PAM4 (SECQ), lane under Test			3.4		dB	
OMAouter of each aggressor lane			4.2		dBm	
LOS Assert		-15			dBm	
LOS De-Assert				-8.9	dBm	
LOS Hysteresis			1.5		dB	

Notes:

1. Receiver sensitivity (OMAouter), per lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.

Digital Diagnostic Monitoring Accuracy (Under Recommended Operating Conditions)

Parameter	Accuracy	Unit	Note
Measured transceiver case temperature	±3	°C	
Measured transceiver supply voltage	±5	%	
Measured Tx bias current	±10	%	
Measured Tx output power	±3	dB	
Measured Rx received average optical power	±3	dB	

Pin Assignment**Top Side (viewed from top)**

60	GND	
59	TX1p	
58	TX1n	
57	GND	
56	TX3p	
55	TX3n	
54	GND	
53	TX5p	
52	TX5n	
51	GND	
50	TX7p	
49	TX7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/RSTn	
43	GND	
42	RX8n	
41	RX8p	
40	GND	
39	RX6n	
38	RX6p	
37	GND	
36	RX4n	
35	RX4p	
34	GND	
33	RX2n	
32	RX2p	
31	GND	

----- Module Card Edge -----

Bottom Side (viewed from bottom)

	GND	1
	TX2p	2
	TX2n	3
	GND	4
	TX4p	5
	TX4n	6
	GND	7
	TX6p	8
	TX6n	9
	GND	10
	TX8p	11
	TX8n	12
	GND	13
	SCL	14
	VCC	15
	VCC	16
	LPWn/PRSn	17
	GND	18
	RX7n	19
	RX7p	20
	GND	21
	RX5n	22
	RX5p	23
	GND	24
	RX3n	25
	RX3p	26
	GND	27
	RX1n	28
	RX1p	29
	GND	30

Pinout of Connector Block on Host Board

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.

TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3 V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3 V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in OSFP Specification.
VCC	power	3.3 V power for module.
GND	ground	Module Ground. Logic and power return path.

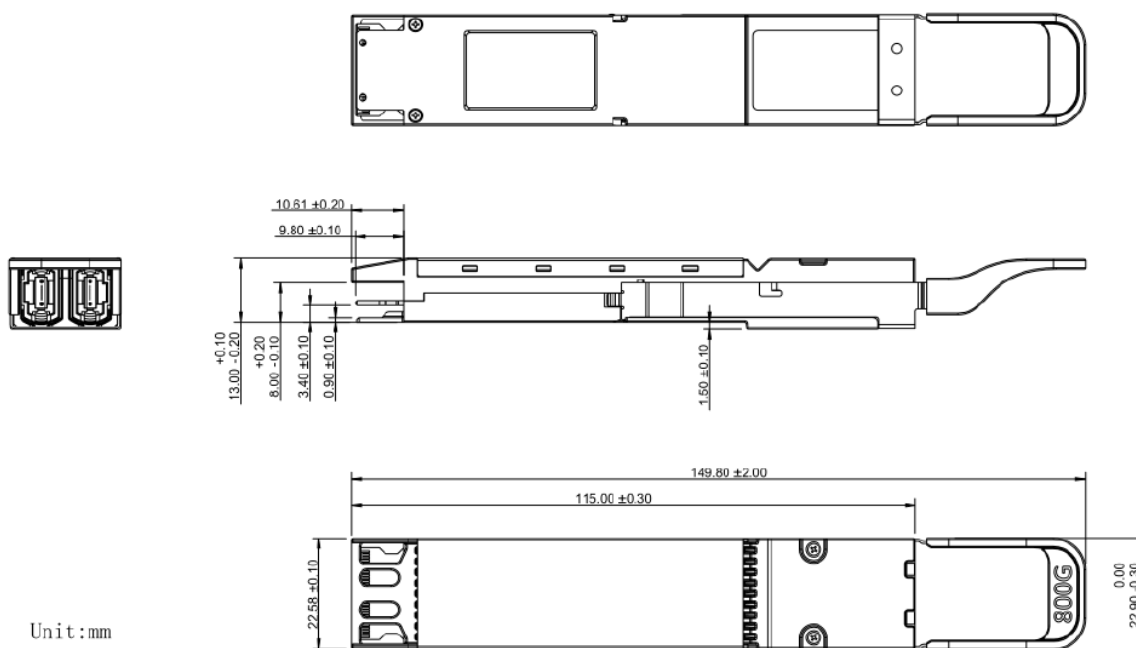
Pin	Symbol	Logic	Description	Notes
1	GND		Ground	
2	TX2p	CML-I	Transmitter Data Non-Inverted	
3	TX2n	CML-I	Transmitter Data Inverted	
4	GND		Ground	
5	TX4p	CML-I	Transmitter Data Non-Inverted	
6	TX4n	CML-I	Transmitter Data Inverted	
7	GND		Ground	
8	TX6p	CML-I	Transmitter Data Non-Inverted	
9	TX6n	CML-I	Transmitter Data Inverted	
10	GND		Ground	
11	TX8p	CML-I	Transmitter Data Non-Inverted	
12	TX8n	CML-I	Transmitter Data Inverted	
13	GND		Ground	
14	SCL	LVC MOS-I/O	2-wire Serial interface clock	1
15	VCC		+3.3 V Power	
16	VCC		+3.3 V Power	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	2
18	GND		Ground	
19	RX7n	CML-O	Receiver Data Inverted	
20	RX7p	CML-O	Receiver Data Non-Inverted	
21	GND		Ground	
22	RX5n	CML-O	Receiver Data Inverted	
23	RX5p	CML-O	Receiver Data Non-Inverted	

24	GND		Ground	
25	RX3n	CML-O	Receiver Data Inverted	
26	RX3p	CML-O	Receiver Data Non-Inverted	
27	GND		Ground	
28	RX1n	CML-O	Receiver Data Inverted	
29	RX1p	CML-O	Receiver Data Non-Inverted	
30	GND		Ground	
31	GND		Ground	
32	RX2p	CML-O	Receiver Data Non-Inverted	
33	RX2n	CML-O	Receiver Data Inverted	
34	GND		Ground	
35	RX4p	CML-O	Receiver Data Non-Inverted	
36	RX4n	CML-O	Receiver Data Inverted	
37	GND		Ground	
38	RX6p	CML-O	Receiver Data Non-Inverted	
39	RX6n	CML-O	Receiver Data Inverted	
40	GND		Ground	
41	RX8p	CML-O	Receiver Data Non-Inverted	
42	RX8n	CML-O	Receiver Data Inverted	
43	GND		Ground	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	2
45	VCC		+3.3 V Power	
46	VCC		+3.3 V Power	
47	SDA	LVC MOS-I/O	2-wire Serial interface data	1
48	GND		Ground	
49	TX7n	CML-I	Transmitter Data Inverted	
50	TX7p	CML-I	Transmitter Data Non-Inverted	
51	GND		Ground	
52	TX5n	CML-I	Transmitter Data Inverted	
53	TX5p	CML-I	Transmitter Data Non-Inverted	
54	GND		Ground	
55	TX3n	CML-I	Transmitter Data Inverted	
56	TX3p	CML-I	Transmitter Data Non-Inverted	
57	GND		Ground	
58	TX1n	CML-I	Transmitter Data Inverted	
59	TX1p	CML-I	Transmitter Data Non-Inverted	

60	GND		Ground	
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Notes:

1. Open-Drain with pull-up resistor on Host
2. See pin description for required circuit

Package Dimensions**Ordering Information**

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-OR8-DR4X2-C	OSFP-RHS	106.25 Gb/s (PAM4) per lane	500 m	0 °C to 70 °C	800G Ethernet	DDM RoHS

Modification History

Revision	Date	Description	Originator	Review	Approve
V1.0	16-Oct-2025	New Issue	Jason Hou	Wayne Liao	Tom Tang

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