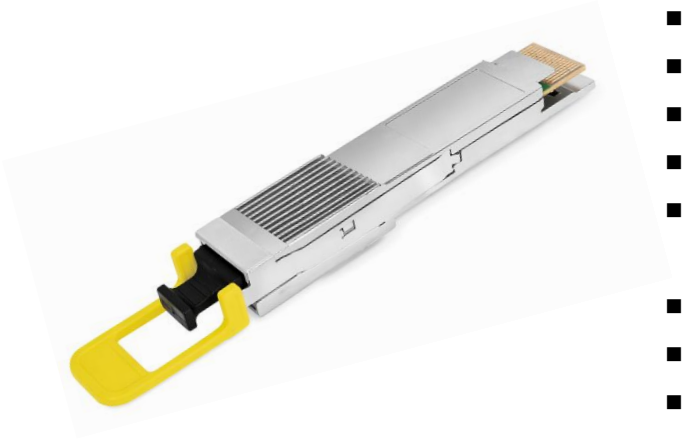
WAVESPLITTER™
TECHNOLOGIES, INC.

Data Sheet

400G QSFP-DD DR4 500m Transceiver Module
P/N: WST-QD4-DR4-C



Features:

- QSFP-DD form factor
- 400 Gb/s aggregate data rate
- Electrical: 8 x 53.125 Gb/s PAM4
- Optical: 4 x 106.25 Gb/s PAM4
- 4-lane parallel EML and PIN photodiode receivers with TIAs
- MPO-12/APC optical connector
- DR4 (500 m) optical interface over single-mode fiber with host-side KP4 FEC
- Hot pluggable
- Single 3.3 V power supply
- Power consumption: Max. 9.5 W
- Operating case temperature: 0 °C to +70 °C
- Digital diagnostic monitoring support

Applications:

- 400 Gigabit Ethernet or InfiniBand links over single-mode fiber
- Data center interconnect applications
- Switch-to-switch and switch-to-router interconnections

Standards:

- IEEE 802.3cn and IEEE 802.3bs compliant
- QSFP-DD compliant
- CMIS 5.2 management interface compliant
- RoHS compliant

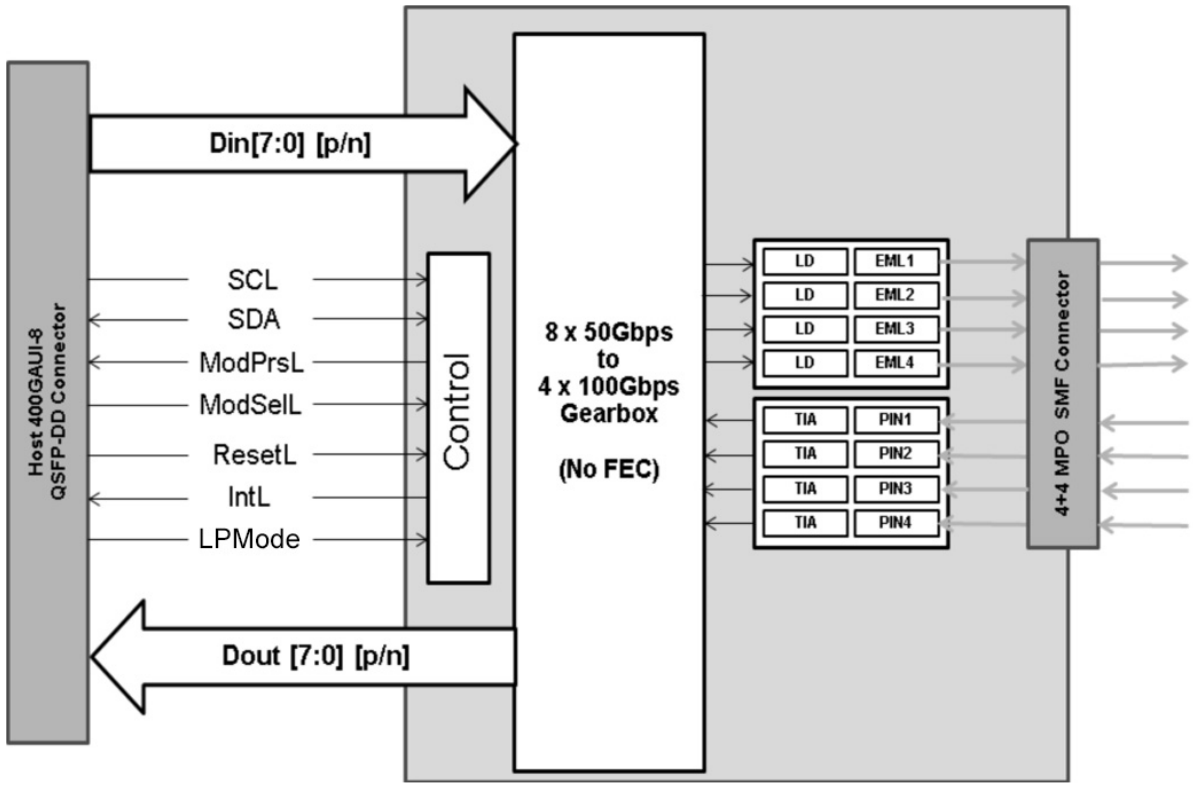
Description

The WST-QD4-DR4-C module is a 400Gb/s QSFP-DD optical transceiver module designed for datacenter-reach single-mode fiber (SMF) transmission. It provides eight electrical lanes operating at 53.125 Gb/s PAM4 signaling and supports a DR4 optical interface for transmission distances up to 500 m over SMF.

The module integrates optical and electrical components within a QSFP-DD form factor and uses MPO-12/APC connector for optical connectivity. The transmitters are based on 1310 nm EML and the receivers use PIN photodiodes with TIAs, optimized for datacenter-reach SMF applications.

Functional Description

The WST-QD4-DR4-C module converts 8 x 53.125 Gb/s PAM4 electrical input signals into optical outputs through integrated transmit circuitry and EML laser drivers, enabling 400 Gigabit Ethernet or InfiniBand links over SMF. The optical interface consists of 4 optical lanes using MPO-12/APC connector. On the receive side, incoming optical signals are converted into electrical signals through PIN photodetectors and receiver circuitry. The module is designed for operation in systems employing host-side KP4 forward error correction (FEC) to meet link performance requirements. The module supports digital diagnostic monitoring (DDM) through the QSFP-DD management interface, enabling monitoring of key operating parameters.



Block diagram of transmit/receive paths

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity	RH	5	85	%	
Receiver Damage Threshold (per lane)			+5	dBm	1

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level. The receiver does not have to operate correctly at this input power.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical Signal Rate (per lane)		53.125 ± 100 ppm			Gb/s	PAM4
Optical Signal Rate (per lane)		106.25 ± 100 ppm			Gb/s	PAM4
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T_C	0		70	°C	
Supply Current	I_{CC}			2.88	A	
Power Consumption	P_C			9.5	W	
Link Distance (G.652)	DI	2		500	m	

Optical Characteristics (Under Recommended Operating Conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Signaling speed (per lane)		106.25 ± 100 ppm			Gb/s	
Modulation format		PAM4				
Lane wavelengths	λ	1304.5	1310	1317.5	nm	
Average launch power (per lane)	P	-2.9		4	dBm	1
OMAouter (per lane)	P_{OMA}	-0.8		4.2	dBm	2
Launch power in OMAouter minus TDECQ (per lane)		-2.2				
Transmitter and dispersion eye closure for PAM4 (TDECQ) (per lane)				3.4	dB	
TDECQ – 10log10(*C*eq)				3.4	dB	3
Side-mode suppression ratio (SMSR)		30			dB	
Extinction ratio (per lane)	ER	3.5			dB	
Average launch power of OFF transmitter (per lane)	P_{off}			-15	dBm	
Transmitter transition time (each lane)				17	ps	
RIN21OMA	RIN			-136	dB/Hz	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26		4
Receiver						
Signaling speed (per lane)		106.25 ± 100 ppm			Gb/s	
Modulation format		PAM4				
Lane wavelengths	λ	1304.5	1310	1317.5	nm	
Average receive power (per lane)		-5.9		4	dBm	5
Receive power (OMAouter) (per lane)	R_{OMA}			4.2	dBm	
Receiver Reflectance				-26	dB	

Receiver sensitivity (OMAouter) (per lane)	SEN	Max(-3.9, -5.3 +SECQ)			dBm	6
Stressed receiver sensitivity (OMAouter) (per lane)	SEN			-1.9		7
Conditions of stressed receiver sensitivity test:						8
Stressed eye closure for PAM4 (SECQ), lane under test		3.4			dB	
SECQ–10*log10(Ceq) (max), lane under test		3.4			dB	
OMAouter of each aggressor lane		4.2			dBm	
LOS Assert		-26			dBm	
LOS De-Assert				-8	dBm	9
LOS Hysteresis		0.5			dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of <4.5 dB, the POMA(min) must exceed this value.
3. Ceq is a coefficient, which accounts for the reference equalizer noise enhancement.
4. Transmitter reflectance is defined looking into the transmitter.
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. SECQ is the transmitter used to measure the receiver sensitivity. Bit error ratio (BER) less than 2.4×10^{-4}.
7. Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3-2018 clause 124.1.1. SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
9. Ceq is a coefficient defined in 121.8.5.3(IEEE), which accounts for the reference equalizer noise enhancement.

Electrical Characteristics (Under Recommended Operating Conditions)

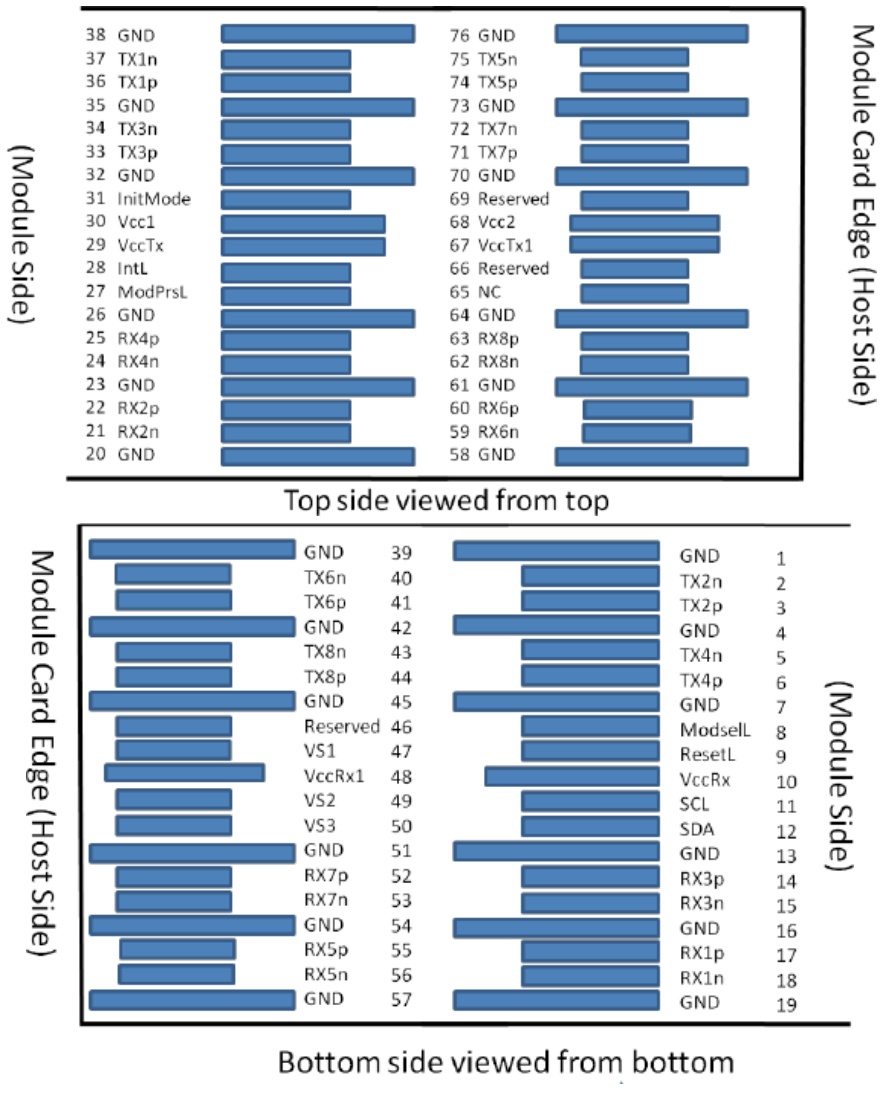
Parameter	Test Point	Min	Typ	Max	Unit	Note
High Speed Electrical Input Characteristics						
Signaling speed (per lane)	TP1	53.125 ± 100 ppm			Gb/s	
Differential pk-pk input voltage tolerance	TP1a	900			mV	1
Differential input return loss (min)	TP1	9.5-0.37*f, 0.01≤f＜8GHz 4.75-7.4*log(f/14), 8≤f＜19GHz			dB	
Differential to common mode input return loss (min)	TP1	22-20*f/25.78, 0.01≤f＜12.89GHz 15-6*f/25.78, 12.89≤f＜19GHz			dB	
Differential termination mismatch	TP1			10	%	
Module stressed input tolerance	TP1a	See IEEE 802.3bs 120E.3.4.1				BER 10^{-5}
Single-ended voltage tolerance	TP1a	-0.4		3.3	V	
DC common-mode voltage	TP1	-0.35		2.85	V	2
High Speed Electrical Output Characteristics						
Signaling speed (per lane)	TP4	53.125 ± 100 ppm			Gb/s	
AC common-mode output voltage (RMS)	TP4			0.0175	V	
Differential peak-to-peak output voltage	TP4			0.9	V	
Near-end ESMW (Eye symmetry mask width)	TP4	0.265			UI	

Near-end Eye height, differential	TP4	0.07			V	
Far-end ESMW (Eye symmetry mask width)	TP4	0.2			UI	
Far-end Eye height, differential	TP4	0.03			V	
Far-end pre-cursor ISI ratio	TP4	-4.5		2.5	%	
Differential output return loss (min)	TP4	9.5-0.37*f, 0.01≤f＜8GHz 4.75-7.4*log(f/14), 8≤f＜19GHz			dB	
Common to differential mode conversion return loss (min)	TP4	22-20*f/25.78, 0.01≤f＜12.89GHz 15-6*f/25.78, 12.89≤f＜19GHz			dB	
Differential termination mismatch	TP4			10	%	
Transition time (20% to 80%)	TP4	9.5			ps	
DC common mode voltage	TP4	-0.35		2.85	V	2

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Pin Assignment



Pin out of Connector Block on Host Board

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VCC Rx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VCC Tx	+3.3 V Power Supply Transmitter	2B	2
30		VCC1	+3.3 V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1	1

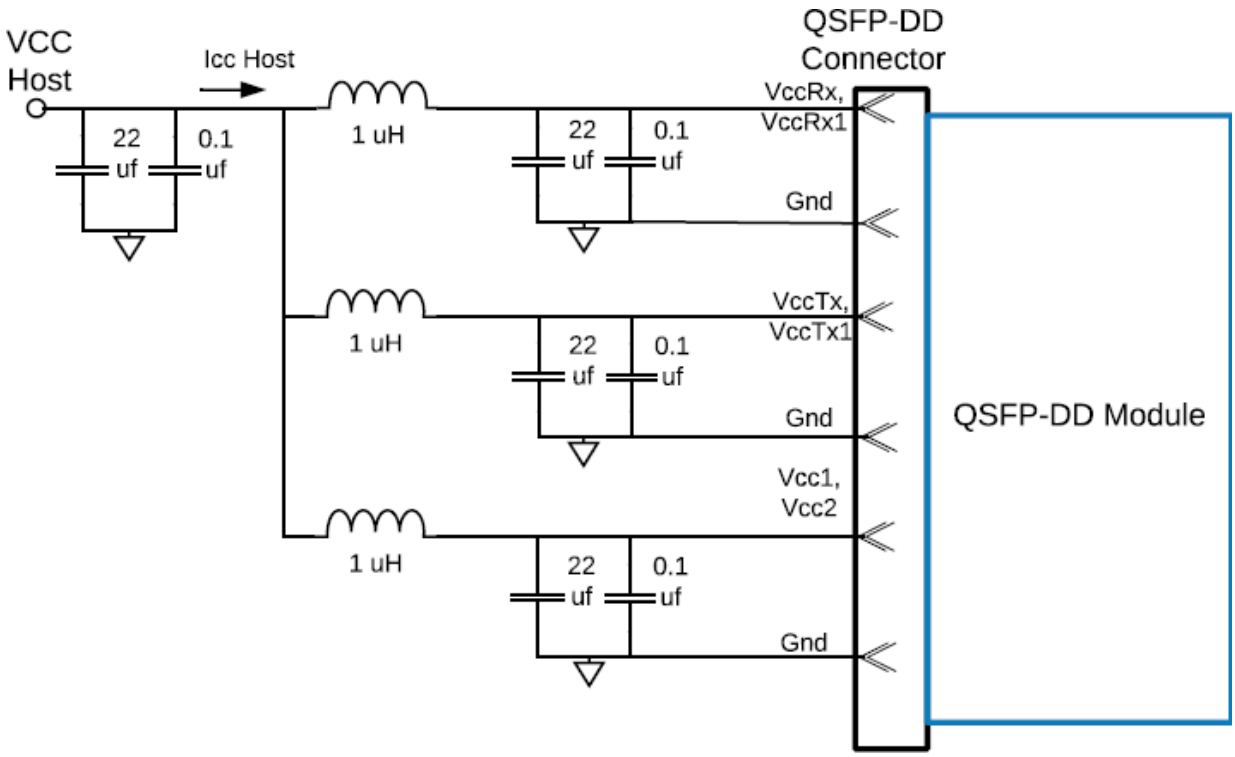
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1B	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VCC Tx1	+3.3 V Power Supply Transmitter	2A	2
68		VCC2	+3.3 V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input (N/C within module)	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	

72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

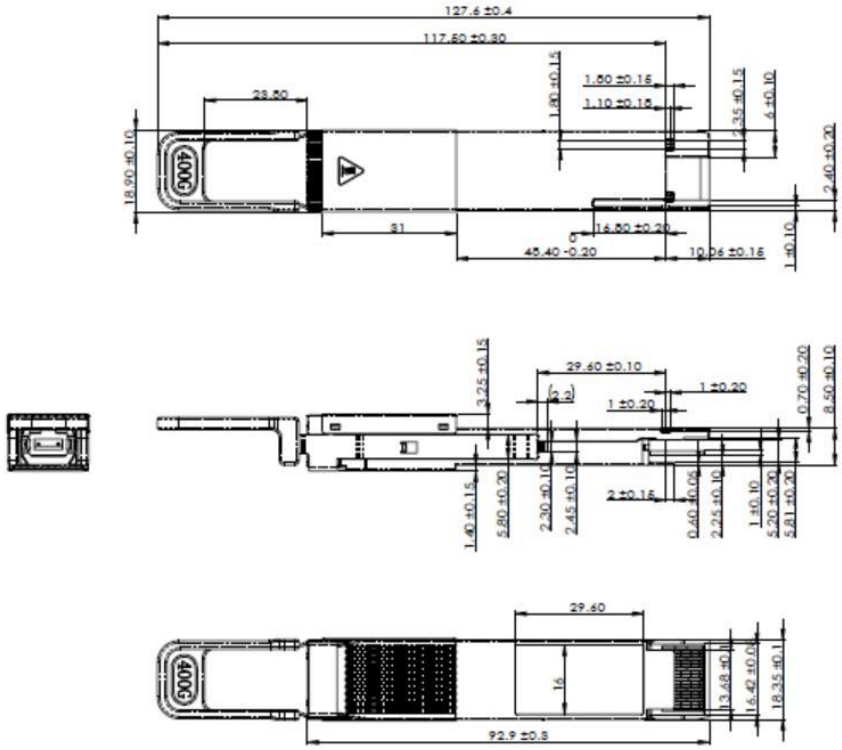
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed above. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Recommended Power Supply Filter



Package Dimensions



(Unit: mm)

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-QD4-DR4-C	**QSFP-DD**	**106.25 Gb/s (PAM4) per optical lane**	**500 m**	**0 °C to 70 °C**	**400G Ethernet or InfiniBand**	**DDM RoHS**

Modification History

Revision	Date	Description	Originator	Review	Approve
V1.0	3-Jun-2024	New Issue	Henry Chung	Wayne Liao	Tom Tang

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