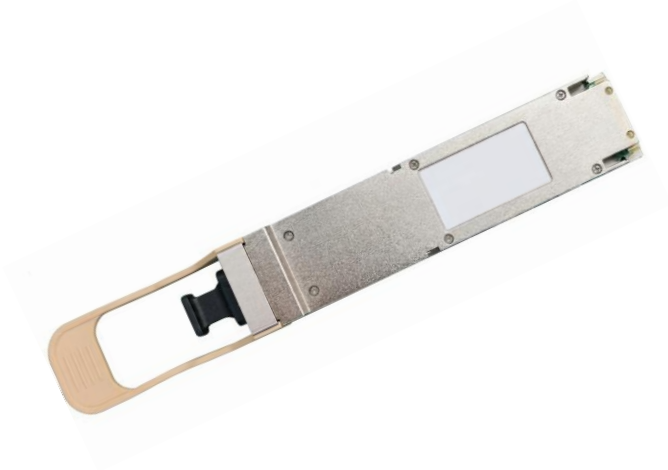
400G OSFP-RHS VR4 50 m Transceiver Module
P/N: WST-OR4-VR4-C



Features:

- Supports aggregate data rate up to 425 Gbps
- Optical interface: 106.25 Gbps PAM4 × 4 lanes
- Electrical interface: 106.25 Gbps PAM4 × 4 lanes
- Parallel 4 optical lanes
- 850 nm VCSEL transmitter and photodetector receiver
- Digital diagnostic monitoring functions supported via CMIS 5.0 management interface
- Transmission distance up to 30 m over OM3 MMF or 50 m over OM4 MMF with FEC
- MPO-12/APC optical interface
- Single +3.3 V power supply
- Low power consumption: 8.5 W max.
- Operating case temperature:
  Commercial: 0 ˚C to 70 ˚C
- RoHS compliant

Standard:

- Compliant with IEEE 802.3db
- Compliant with IEEE 802.3ck
- Compliant with OSFP Multi-Source Agreement (MSA), OSFP-RHS
- Management interface compliant with CMIS 5.0

Application:

- 400G Ethernet
- InfiniBand
- Breakout applications
- Data center interconnects

Description

The WST-OR4-VR4-C is a high-performance and cost-effective 400G OSFP-RHS VR4 transceiver module supporting an aggregate data rate of 425 Gbps. It supports transmission distance up to 30 m over OM3 Multi-Mode Fiber (MMF) or 50 m over OM4 MMF with FEC. The module is designed for 400G Ethernet, InfiniBand, breakout applications, and data center interconnects.

Functional Description

The transceiver consists of 850 nm VCSEL transmitters, photodetector receivers, and an internal control and management unit. It converts four electrical input lanes into four optical output lanes at 106.25 Gbps PAM4 per lane, providing an aggregate data rate of 425 Gbps. The module supports digital diagnostic monitoring functions via the CMIS 5.0 management interface and incorporates proven VCSEL, receiver, and control circuitry to provide reliable performance with low power consumption and RoHS compliance.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	V_{cc}	-0.4		3.6	V	
Storage Temperature	T_S	-40		85	°C	
Relative Humidity	RH	5		85	%	Non-condensing

Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Electrical Signal Rate, each lane		53.125 ± 100 ppm			GBd	
Optical Signal Rate, each lane		53.125 ± 100 ppm			GBd	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			2.6	A	
Operating Case Temp.	Tc	0		70	°C	
Power Consumption	Pc			8.5	W	
Link Distance with OM3	D1			30	m	
Link Distance with OM4	D2			50	m	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling rate per lane (PAM4 encoded)	TP1	-100 ppm	53.125	+100 ppm	GBd	
Differential peak-peak input voltage tolerance	TP1a	750			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance	TP1a	-0.4		3.3	V	
DC common-mode voltage	TP1	-0.35		2.85	V	
Receiver						
Signaling rate per lane (PAM4 Encoded)	TP4	-100 ppm	53.125	+100 ppm	GBd	

AC common-mode output voltage (RMS)	TP4			25	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	 mV	
Near-end Eye height, differential	TP4	70			mV	
Far-end Eye height, differential	TP4	30			mV	
Far end pre-cursor ratio	TP4	-4.5		2.5	%	
Differential Termination Mismatch	TP4			10	%	
Transition Time (min, 20% to 80%)	TP4	9.5			ps	
DC common-mode voltage tolerance	TP4	-0.25		2.85	V	1

Note:

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

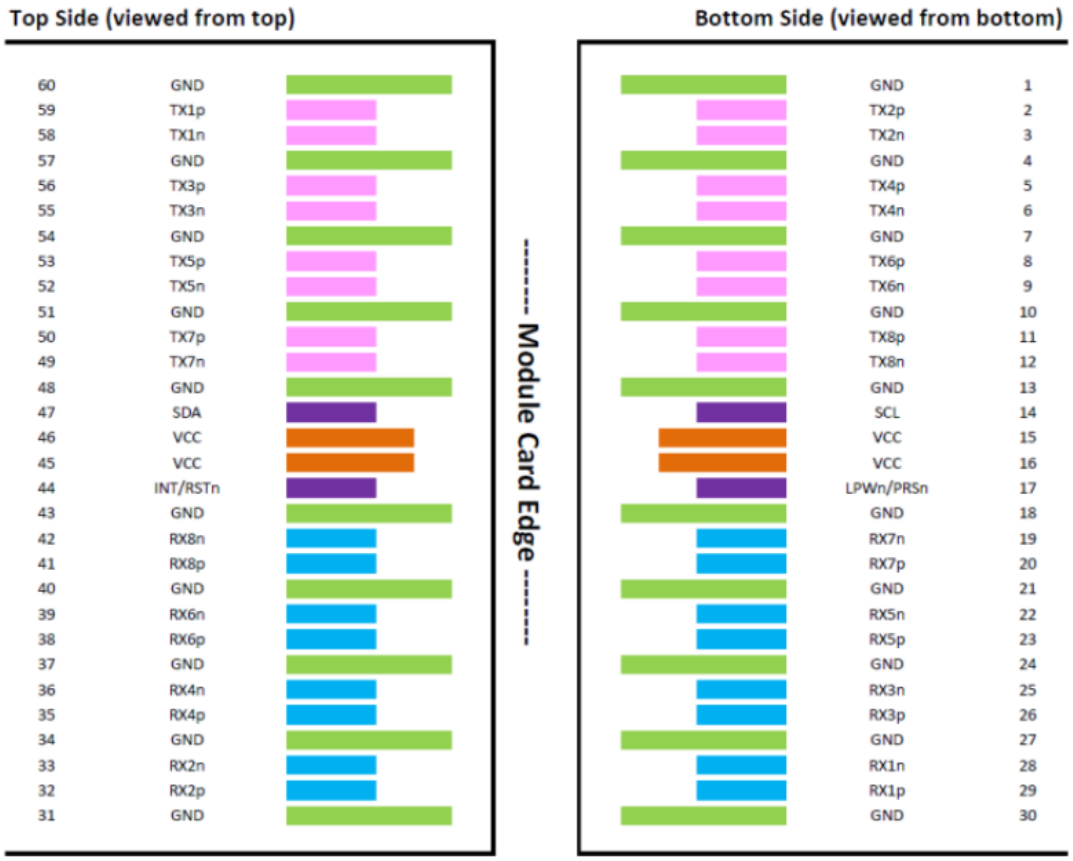
Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Transmitter						
Signaling rate per lane (range)		-100 ppm	53.125	+100 ppm	GBd	
Modulation format			PAM4			
Center wavelength (range)	λ	844	850	868	nm	
RMS spectral width				0.65	nm	1
Average launch power, each lane	P	-4.6		4	dBm	2
OMAouter, each lane for max (TECQ, TDECQ) ≤1.8 dB for 1.8 < max (TECQ, TDECQ) ≤ 4.4 dB	P_{OMA}	-2.6 -4.4+ max (TECQ, TDECQ)		3.5 3.5	dBm	2,3
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				4.4	dB	
Transmitter power excursion, each lane (max)				2.3	dBm	
Extinction ratio, each lane	ER	2.5			dB	
Average launch power of OFF transmitter, each lane	P_{off}			-30	dBm	
RIN21OMA	RIN			-132	dB/Hz	

Encircled flux		≥ 86% at 19 μm ≤ 30% at 4.5 μm				4
Receiver						
Signaling rate per lane (range)		-100 ppm	53.125	+100 ppm	GBd	
Modulation format		PAM4				
Receiver wavelength (range)	λ	842	-	948	nm	
Damage Threshold, each lane		5			dBm	5
Average receive power, each lane		-6.4		4	dBm	2,6
Receive power , each lane (OMAouter)	R_{OMA}			3.5	dBm	
Receiver reflectance	Rr			-15	dB	
Receiver Sensitivity (OMA) per Lane max for TECQ ≤1.8 dB for 1.8 < TECQ ≤ 4.4 dB	SEN			-4.6 -6.4+TECQ	dBm dBm	7
LOS Assert		-20			dBm	
LOS De-Assert				-9	dBm	
LOS Hysteresis		0.5			dB	
Conditions of stressed receiver sensitivity test:						8
Stressed eye closure for PAM4 (SECQ), lane under test		4.4			dB	
OMAouter of each aggressor lane		3.5			dBm	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Editor's note: Based on stressed receiver sensitivity of -2 dBm, and may increase by up to 0.4 dB based on the choice of stressed receiver sensitivity
3. If the TDECQ <1.4 dB, the OMA (min) has to exceed this value.
4. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.
5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Pin Assignment



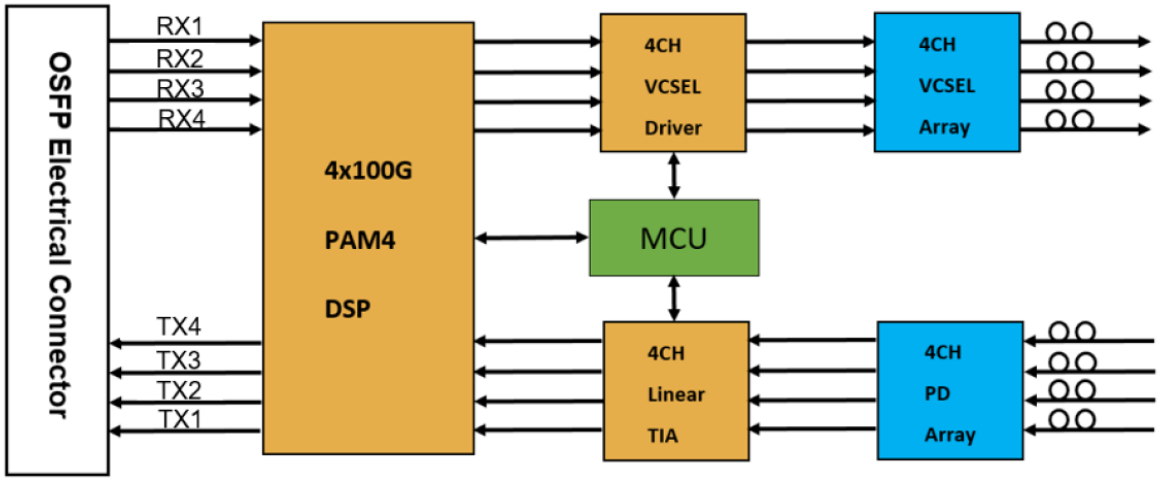
Pin out of Connector Block on Host Board

PIN	Name	Logic	Description	Direction	Notes
1	GND		Ground		
2	TX2p	CML-I	Transmitter Data Non-Inverted	Input from Host	
3	TX2n	CML-I	Transmitter Data Inverted	Input from Host	
4	GND		Ground		
5	TX4p	CML-I	Transmitter Data Non-Inverted	Input from Host	
6	TX4n	CML-I	Transmitter Data Inverted	Input from Host	
7	GND		Ground		
8	TX6p	CML-I	Transmitter Data Non-Inverted	Input from Host	Unused in 400G Mode
9	TX6n	CML-I	Transmitter Data Inverted	Input from Host	Unused in 400G Mode

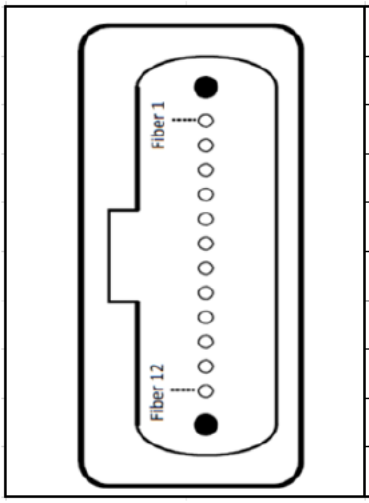
10	GND		Ground		
11	TX8p	CML-I	Transmitter Data Non-Inverted	Input from Host	Unused in 400G Mode
12	TX8n	CML-I	Transmitter Data Inverted	Input from Host	Unused in 400G Mode
13	GND		Ground		
14	SCL	LVCMOS-I/O	2-wire Serial interface clock	Bi-directional	
15	VCC		+3.3V Power supply	Power from Host	
16	VCC		+3.3V Power supply	Power from Host	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	Bi-directional	
18	GND		Ground		
19	RX7n	CML-O	Receiver Data Inverted	Output to Host	Unused in 400G Mode
20	RX7p	CML-O	Receiver Data Non-Inverted	Output to Host	Unused in 400G Mode
21	GND		Ground		
22	RX5n	CML-O	Receiver Data Inverted	Output to Host	Unused in 400G Mode
23	RX5p	CML-O	Receiver Data Non-Inverted	Output to Host	Unused in 400G Mode
24	GND		Ground		
25	RX3n	CML-O	Receiver Data Inverted	Output to Host	
26	RX3p	CML-O	Receiver Data Non-Inverted	Output to Host	
27	GND		Ground		
28	RX1n	CML-O	Receiver Data Inverted	Output to Host	
29	RX1p	CML-O	Receiver Data Non-Inverted	Output to Host	
30	GND		Ground		
31	GND		Ground		
32	RX2p	CML-O	Receiver Data Non-Inverted	Output to Host	
33	RX2n	CML-O	Receiver Data Inverted	Output to Host	
34	GND		Ground		

35	RX4p	CML-O	Receiver Data Non-Inverted	Output to Host	
36	RX4n	CML-O	Receiver Data Inverted	Output to Host	
37	GND		Ground		
38	RX6p	CML-O	Receiver Data Non-Inverted	Output to Host	Unused in 400G Mode
39	RX6n	CML-O	Receiver Data Inverted	Output to Host	Unused in 400G Mode
40	GND		Ground		
41	RX8p	CML-O	Receiver Data Non-Inverted	Output to Host	Unused in 400G Mode
42	RX8n	CML-O	Receiver Data Inverted	Output to Host	Unused in 400G Mode
43	GND		Ground		
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	Bi-directional	
45	VCC		+3.3V Power supply	Power from Host	
46	VCC		+3.3V Power supply	Power from Host	
47	SDA	LVCMOS-I/O	2-wire Serial interface data	Bi-directional	
48	GND		Ground		
49	TX7n	CML-I	Transmitter Data Inverted	Input from Host	Unused in 400G Mode
50	TX7p	CML-I	Transmitter Data Non-Inverted	Input from Host	Unused in 400G Mode
51	GND		Ground		
52	TX5n	CML-I	Transmitter Data Inverted	Input from Host	Unused in 400G Mode
53	TX5p	CML-I	Transmitter Data Non-Inverted	Input from Host	Unused in 400G Mode
54	GND		Ground		
55	TX3n	CML-I	Transmitter Data Inverted	Input from Host	
56	TX3p	CML-I	Transmitter Data Non-Inverted	Input from Host	
57	GND		Ground		
58	TX1n	CML-I	Transmitter Data Inverted	Input from Host	
59	TX1p	CML-I	Transmitter Data Non-Inverted	Input from Host	
60	GND		Ground		

Recommended Block Diagram



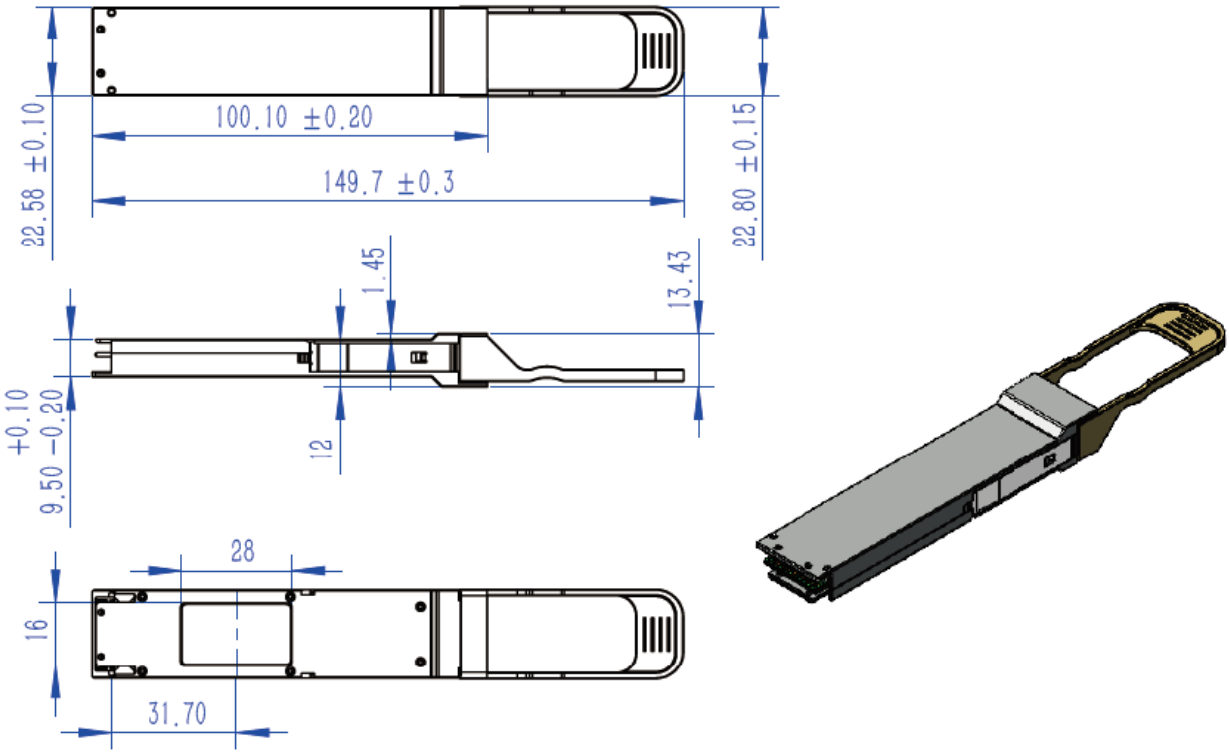
Optical Interface Lanes and Assignment



Fiber	Lane
1	RX1
2	RX2
3	RX3
4	RX4
5678	
9	TX4
10	TX3
11	TX2
12	TX1

Mechanical Drawing

OSFP-RHS Type:



（Unit：mm）

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-OR4-VR4-C	OSFP-RHS	53.125 GBd (PAM4) per optical lane	30 m over OM3 MMF / 50 m over OM4 MMF	0 °C to 70 °C	400G Ethernet	DDM RoHS

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	19-Sep-2023	New Release	Jason Hou	Wayne Liao	Tom Tang

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