

200G QSFP56 SR4 100m Transceiver Module WST-QS56-SR4 Series



Applications:

- 200G Ethernet (200GBASE-SR4)
- Data center interconnect (DCI)
- High-speed switch and router connections

Features:

- QSFP56 hot-pluggable form factor
- 4-channel PAM4 modulation, 26.5625 GBd per lane
- Supports 200GBASE-SR4 up to 100 m over OM4 multimode fiber
- +3.3 V single power supply
- Power dissipation < 6 W
- MPO-12 / APC or UPC optical connector
- Digital Diagnostics Monitoring (DDM) support
- Operating case temperature: 0 °C to 70 °C
- RoHS compliant

Standards:

- IEEE 802.3cd 200GBASE-SR4
- QSFP56 MSA compliant
- CMIS Rev. 4.0 compliant for SR4-C and SR4UC
- SFF-8636 compliant for SR4F-C and SR4FUC

Product Description

The WST-QS56-SR4 series are 200G QSFP56 optical transceiver modules designed for short-reach data communication and interconnect applications. The module supports 4-channel PAM4 modulation operating at 26.5625 GBd per lane, enabling an aggregate data rate of 200 Gb/s. The optical interface utilizes 4 parallel multimode fiber lanes over OM4 with a maximum reach of up to 100 m. The electrical interface complies with QSFP56 standards, providing high-speed connectivity between host systems and optical links.

The module integrates a DSP, VCSEL drivers, and photodiodes to ensure reliable transmission and reception signals. It supports Digital Diagnostics Monitoring (DDM) for real-time performance monitoring. Two management interface options are available: WST-QS56-SR4-C / WST-QS56-SR4UC (CMIS compliant) and WST-QS56-SR4F-C / WST-QS56-SR4FUC (SFF-8636 compliant).

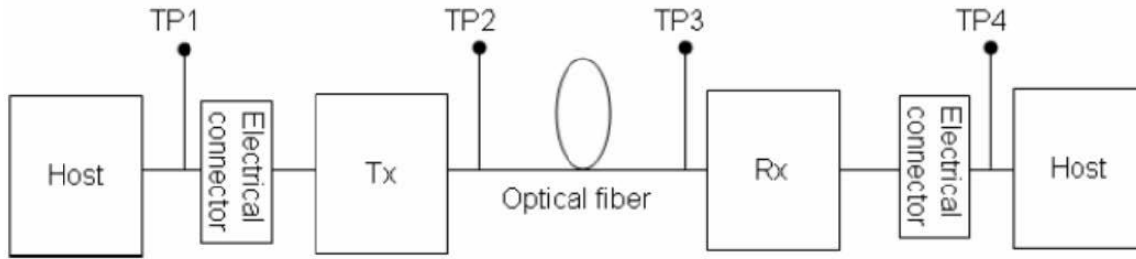


Fig.1 Test compliance points

Absolute Maximum Ratings

Exceeding the limits below may damage the optical transceiver module permanently.

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Maximum Supply Voltage	V _{cc}	-0.5		3.6	V	
Storage Temperature	T _{sto}	-40		85	°C	
Relative Humidity	RH	5		85	%	1
Receiver Damage Threshold per Lane		5			dBm	

Notes:

1. No-condensing.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Case Operating Temperature	T _{op}	0		70	°C	
Supply Voltage	V _{cc}	3.135	3.3	3.465	V	
Power Consumption	P _{Con}			6	W	
Transmission Distance				100	m	
Coupled fiber	OM4					

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transmitter						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm			Gbps	
Differential data input voltage per lane	V _{in,pp,diff}	900			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage	EH	-350		2850	mV	
Receiver						
Signaling rate (each lane)	SR	26.5625± 100 ppm			GBd	
Differential output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Near-end Eye height, differential (min)		70			mV	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential(min)		30			mV	
Differential termination mismatch				10	%	
Transition time (20% to 80%)	Tr, Tf	9.5			ps	
DC common mode voltage		-350		2850	mV	

Optical Characteristics

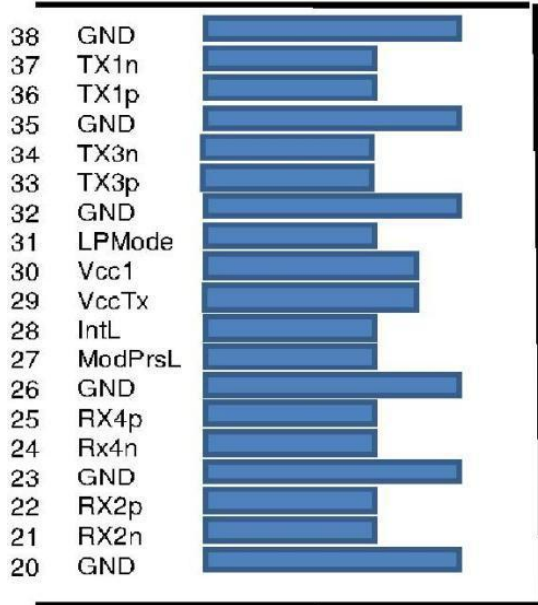
Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transmitter						
Signaling Speed per Lane		26.5625 ± 100ppm			GBd	
Modulation format		PAM4				
Lane wavelengths (Range)	λ	840	850	860	nm	
RMS Spectral Width	$\Delta\lambda$			0.6	nm	
Average launch power, each lane	P _{avg}	-6.5		4	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane (max)		-4.5		3	dBm	1
Launch power in OMA _{outer} minus TDECQ (min)		-5.9			dBm	

Transmitter and dispersion eye closure for PAM4(TDECQ), each lane				4.5	dB	
Extinction ratio	ER	3			dB	
Average launch power of OFF transmitter, each lane	P _{off}			-30	dBm	
Transmitter transition time, each lane				34	ps	
Optical return loss tolerance				12	dB	
Receiver						
Signaling Speed per Lane		26.5625 ± 100ppm			GBd	
Modulation format		PAM4				
Lane wavelengths (Range)	λ	840	850	860	nm	
Damage threshold		+5			dBm	
Average receive power, each lane		-8.4		4	dBm	
Receive power (OMA _{outer}), each lane				3	dBm	
Receiver sensitivity (OMA _{outer}), each lane				Max (6.5,SECQ-7.9)	dBm	2
LOS Assert		-30		-10.0	dBm	
LOS De-Assert				-9	dBm	
LOS Hysteresis		0.5			dB	

Notes:

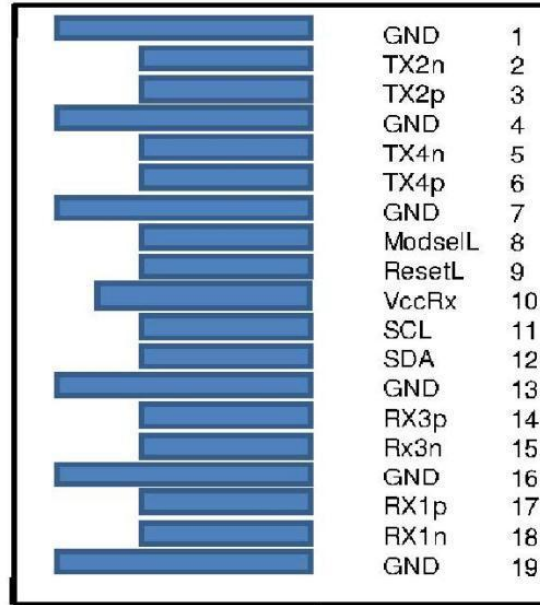
1. Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) must exceed this value.
2. Bit Error Ratio < 2.4x10⁻⁴, Pattern PRBS31Q

Pin Assignment



**Top Side
Viewed From Top**

Module Card Edge



**Bottom Side
Viewed From Bottom**

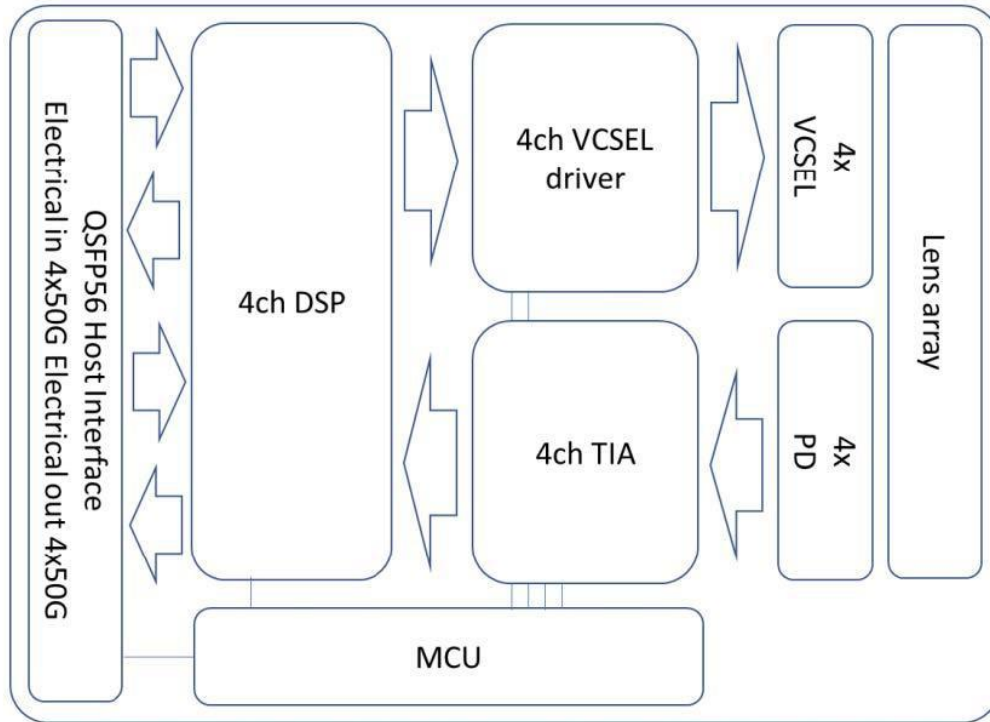
PIN	Symbol	Description	Ref.
1	GND	Ground	1
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	V _{cc} RX	+3.3V Receiver Power Supply Receiver	

11	SCL	2-wire Serial Interface Clock	
12	SDA	2-wire Serial Interface Data	
13	GND	Ground	1
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present, internal pulled down to GND	
28	IntL	Interrupt output, should be pulled up on host board	
29	Vcc TX	+3.3V Transmitter Power Supply	
30	Vcc1	+3.3V Power Supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	1
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	1

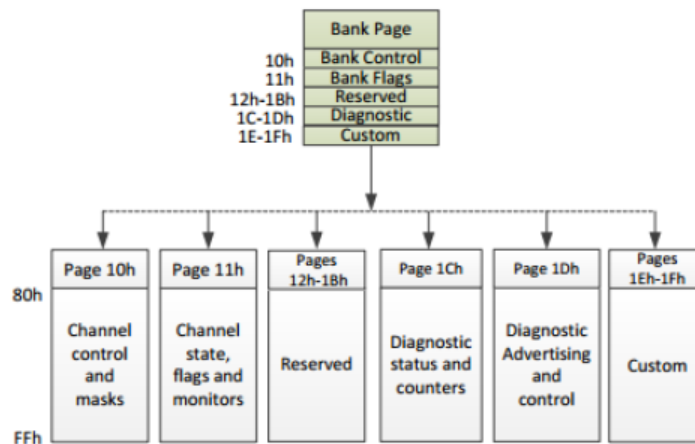
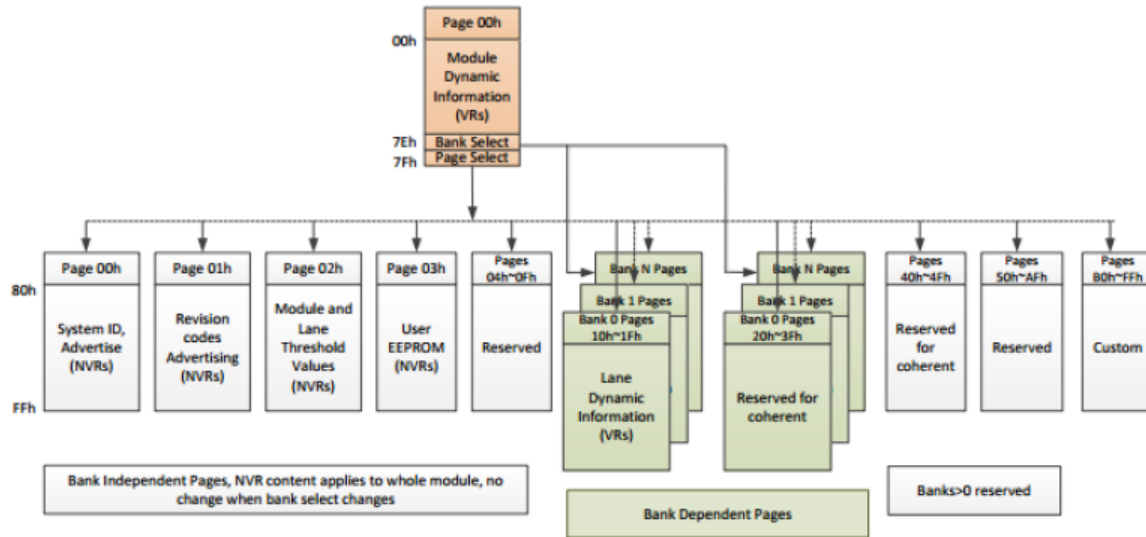
Notes:

1. Circuit ground is internally isolated from chassis ground.

Module Block Diagram



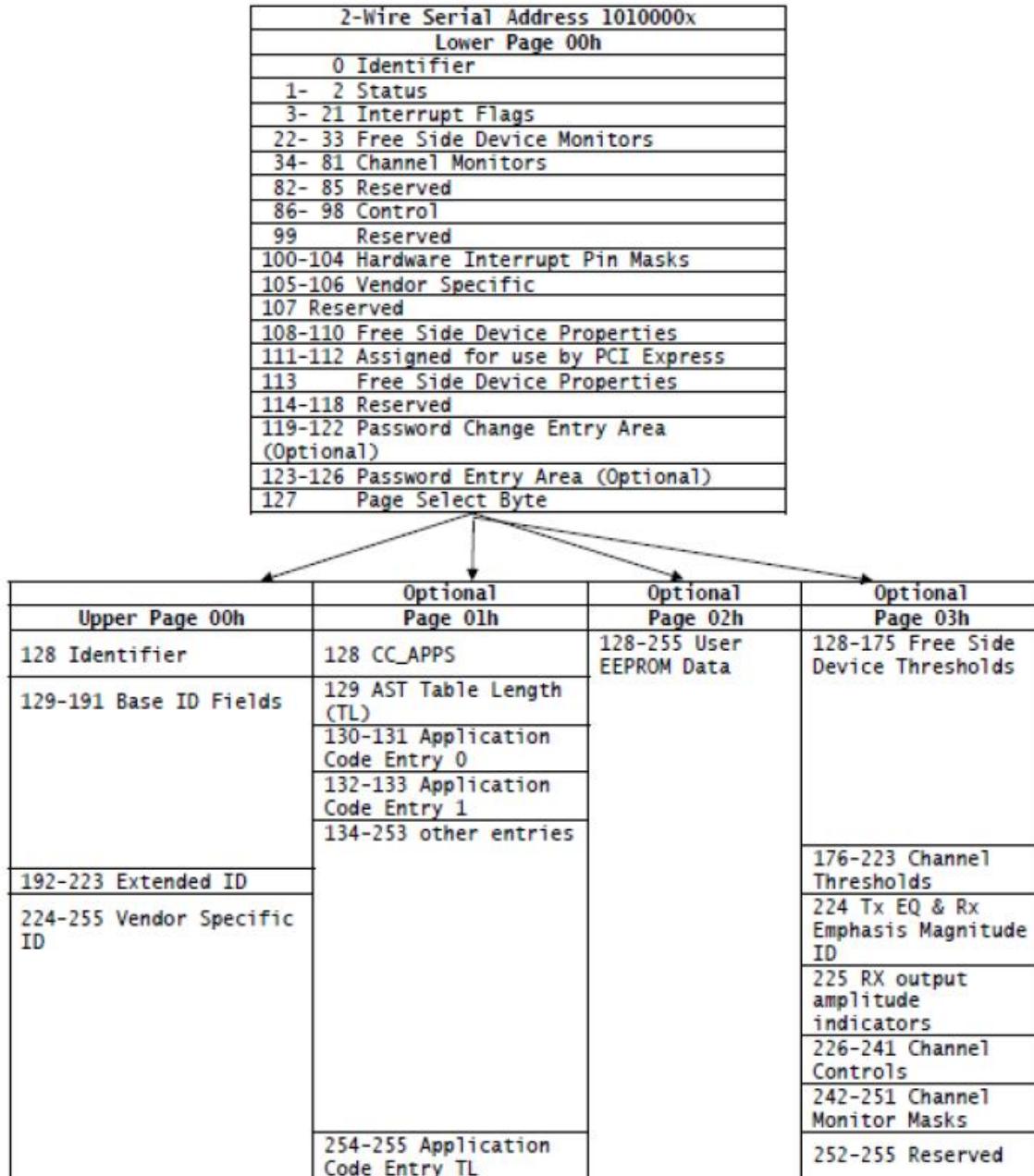
MEMORY MAP for SR4-C and SR4UC, compliant to CMIS Rev. 4.0



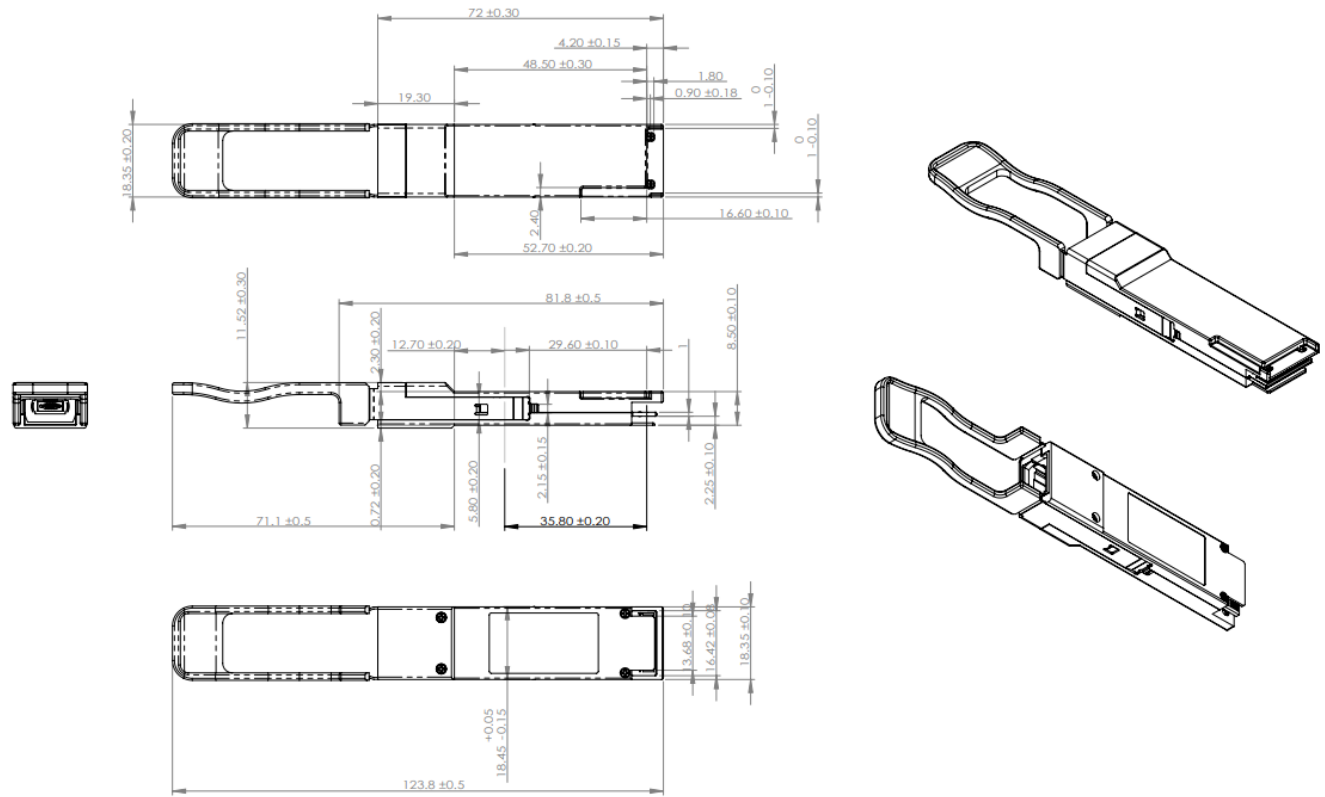
Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

MEMORY MAP for SR4F-C and SR4FUC, compliant to SFF-8636

The memory map is structured as a single address and multiple page approaches, according to the QSFP SFF-8636 SNIA (Storage Networking Industry Association) specification as shown below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification								
	Package	Connector	Data rate per Lane	Laser	Management Interface	Temp	Reach	Application code	Note
WST-QS56-SR4-C	QSFP56	MPO-12 APC	26.5625 GBd	4x50G PAM4 VCSEL	CMIS 4.0	0~70°C	100m via OM4	200GBASE-SR4	DDM RoHS
WST-QS56-SR4UC	QSFP56	MPO-12 UPC	26.5625 GBd	4x50G PAM4 VCSEL	CMIS 4.0	0~70°C	100m via OM4	200GBASE-SR4	DDM RoHS
WST-QS56-SR4F-C	QSFP56	MPO-12 APC	26.5625 GBd	4x50G PAM4 VCSEL	SFF-8636	0~70°C	100m via OM4	200GBASE-SR4	DDM RoHS
WST-QS56-SR4FUC	QSFP56	MPO-12 UPC	26.5625 GBd	4x50G PAM4 VCSEL	SFF-8636	0~70°C	100m via OM4	200GBASE-SR4	DDM RoHS

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	27-May-2025	New Release	Joanne Ni	Ken Cheng	Wayne Liao
V1.1	Apr-21-2026	Add SFF-8636 and APC/UPC type	Henry Chung	Wayne Liao	Tom Tang

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