100G QSFP28 DR1 Transceiver

P/N: WST-QS28-DR-C

Standard:

- Compliant with IEEE 802.3cu
- Compliant with QSFP28 MSA
- Compliant RoHS.

Features:

- Optical Interface: 106.25 Gbps (PAM4)
- Four-lane NRZ electrical host interface at 25.78 Gb/s per lane
- 1310nm EML and PIN design
- Up to 500m over SMF with FEC
- Single 3.3V power supply
- Power consumption: 4W Max
- LC duplex connector
- Operating case temperature: 0 to 70 °C

Applications:

- 100G Ethernet links for data center interconnects over single-mode fiber
- Switch-to-switch and switch-to-router interconnections
- Deployment in systems utilizing 400G DR4 breakout architectures
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Product Description

The WST-QS28-DR-C is a hot-pluggable 100G QSFP28 DR1 optical transceiver for single-mode fiber applications. The module supports a 106.25 Gb/s PAM4 optical interface at 1310 nm and a four-lane 25.78 Gb/s NRZ electrical host interface. A DSP-based signal processing architecture is used to enable conversion between the electrical and optical interfaces.

The optical transmitter uses a 1310 nm EML, and the receiver employs a PIN photodiode. The module supports transmission distances up to 500 meters over G.652 fiber with host-side FEC enabled, operates from a single 3.3 V power supply, and complies with IEEE 802.3cu and QSFP28 MSA requirements.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-40	85	°C	
Operating Case Temperature	Tc	0	70	°C	
Relative Humidity	RH	15	85	%	
Supply Voltage	Vcc	-0.5	3.6	V	
Damage Threshold	THd	5		dBm	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Electrical Signal Rate, each lane		25.78125 ± 100 ppm			Gbps	**NRZ**
Optical Signal Rate		53.125 ± 100 ppm			GBd	**PAM4**
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Operating Case Temp.	Tc			70	°C	
Power Consumption	P			4	W	
Link Distance with G.652		2-	-	500	m	**1**

Notes: 1. FEC is required to be turned on to support maximum transmission distance.

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter						
Signaling rate per lane		25.78125±100ppm			Gb/s	
Differential data input swing per lane	Vin,pp,dif			900	mV	
DC common mode voltage		-350		2850	mV	
Differential termination mismatch				10	%	
Differential input return loss		Per Section 83E.3.3.1, IEEE 802.3bm				
Differential to common mode input return loss		Per Section 83E.3.3.1, IEEE 802.3bm				
Module stressed input test		Per Section 83E.3.4.1, IEEE 802.3bm				
Receiver						
Signaling rate per lane		25.78125±100ppm			Gb/s	
Differential data output swing	Vout,pp			900	mV	
DC common mode voltage		-350		2850	mV	
Common Mode Noise, RMS				17.5	mV	
Differential termination mismatch				10	%	
Eye width		0.57			UI	
Eye height, differential		228			mV	
Vertical eye closure	VEC			5.5	dB	
Transition time (20% to 80%)	tr, tf	12			ps	
Differential output return loss		Per Section 83E.3.1.3, IEEE 802.3bm				
Common to differential mode conversion return loss		Per Section 83E.3.1.3, IEEE 802.3bm				

Note

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics (Under Recommended Operating Conditions)

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Signaling Speed		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Transmitter						
Center Wavelength	λt	1304.5		1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power	P_{AVG}	-2.9		4	dBm	1
Outer Optical Modulation Amplitude (OMA outer)	P_{OMA}	-0.8		4.2	dBm	2
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ)	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Note**
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter	P_{off}			-15	dBm	
RIN15.5OMA	RIN			-136	dB/Hz	
Optical Return Loss Tolerance				15.5	dB	
Transmitter Reflectance				-26	dB	3
Receiver						
Center Wavelength	λr	1304.5		1317.5	nm	
Damage Threshold	THd	5			dBm	4
Average Receive Power		-5.9		4	dBm	5
Receive Power (OMA outer)				4.2	dBm	
Receiver Reflectance				-26	dB	
Receiver Sensitivity (OMA outer)	SEN	max(−3.9,$SECQ$−5.3)			dBm	6
LOS Assert	LOSA	-30		-7.4	dBm	
LOS Deassert	LOSD	-29.5		-6.9	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Note

1. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or TDECQ < 1.1dB for an extinction ratio of < 5dB, the OMA outer (min) must exceed the minimum value specified here.

3. Transmitter reflectance is defined looking into the transmitter.

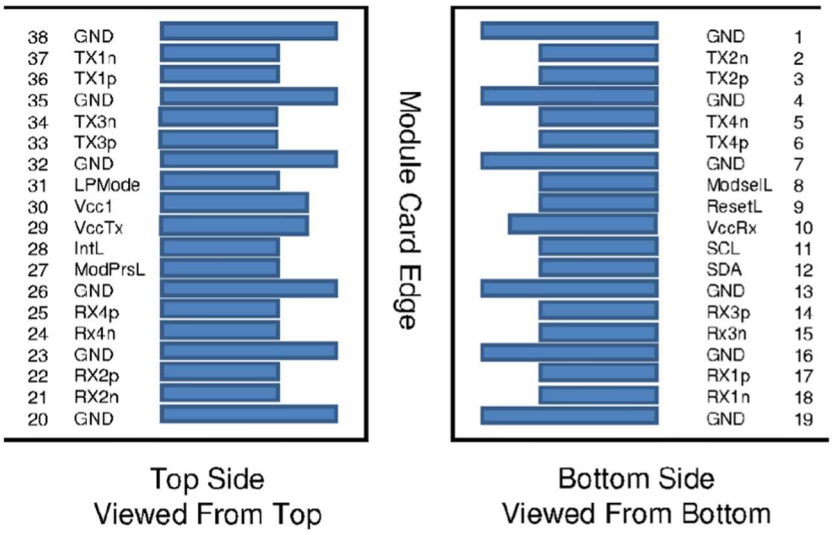
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.

5. Average receive power (min) is informative and not the principal indicator of signal strength. A received power

below this value cannot be compliant; however, a value above this does not ensure compliance.

6. Receiver sensitivity (OMA outer) (max) for 100GBASE-DR is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

Pin Description



Pin	Name	Logic	Description	Notes
1	GND		Ground	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	8
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	8
4	GND		Ground	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	8
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	8
7	GND		Ground	1
8	ModSelL	LVTTL-I	Module Select	3
9	ResetL	LVTTL-I	Module Reset	4
10	Vcc Rx		+3.3V Power Supply Receiver	2
11	SCL	LVCMOS-I/O	2-wire serial interface clock	5
12	SDA	LVCMOS-I/O	2-wire serial interface data	5
13	GND		Ground	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	7
15	Rx3n	CML-O	Receiver Inverted Data Output	7

Pin	Name	Logic	Description	Notes
16	GND		Ground	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	7
18	Rx1n	CML-O	Receiver Inverted Data Output	7
19	GND		Ground	1
20	GND		Ground	1
21	Rx2n	CML-O	Receiver Inverted Data Output	7
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	7
23	GND		Ground	1
24	Rx4n	CML-O	Receiver Inverted Data Output	7
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	7
26	GND		Ground	1
27	ModPrsL	LVTTL-O	Module Present	6
28	IntL/Rx_LOS	LVTTL-O	Interrupt/Rx LOS	
29	Vcc Tx		+3.3V Power supply transmitter	2
30	Vcc1		+3.3V Power supply	2
31	LPMode/Tx_DIS	LVTTL-I	Low Power Mode/Tx Disable	
32	GND		Ground	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	8
34	Tx3n	CML-I	Transmitter Inverted Data Input	8
35	GND		Ground	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data	8
37	Tx1n	CML-I	Transmitter Inverted Data Input	8
38	GND		Ground	1

Note

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA. Recommended host board power supply filtering is shown below.

3. The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newlyselected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4. The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

5. Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1.Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA are a hot plug interface that may support a bus topology.

6. ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

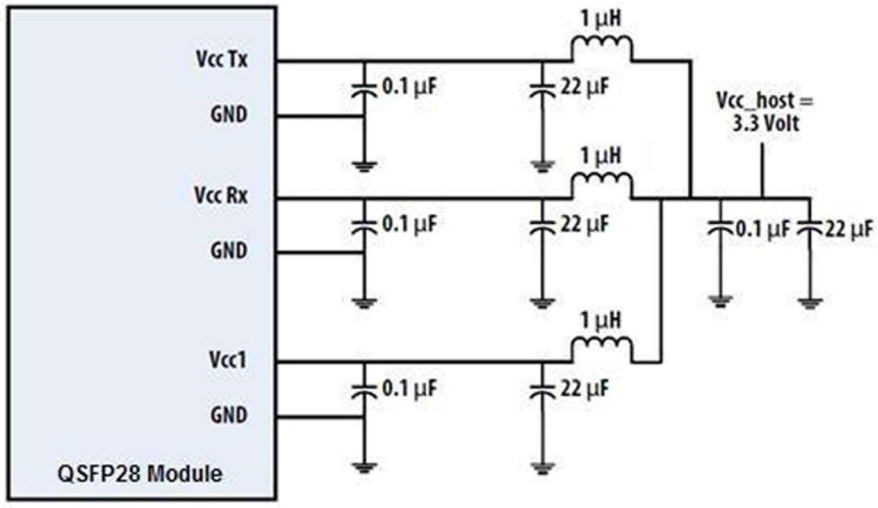
7. Rx(n)(p/n) are module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards.Note: Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a host designed for higher speed operation, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential. Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp. In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to SFF-8636.

8. Tx(n)(p/n) are module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines.

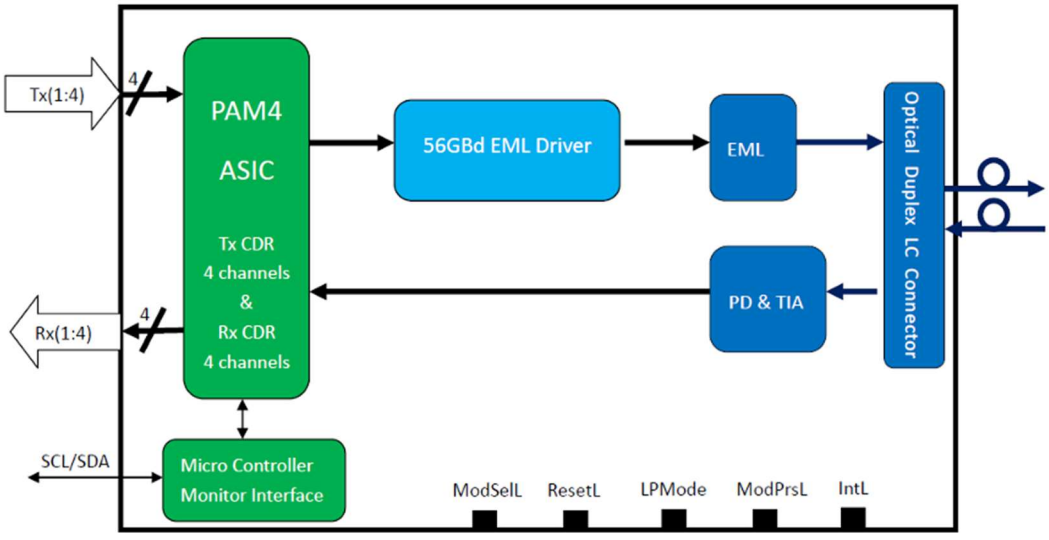
For operation at lower rates, refer to the relevant standards. Due to the possibility of insertion of modules into a host designed for lower speed operation, the damage threshold of the module input shall be at least 1600 mV peak to peak

differential. Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended. In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to SFF- 8636.

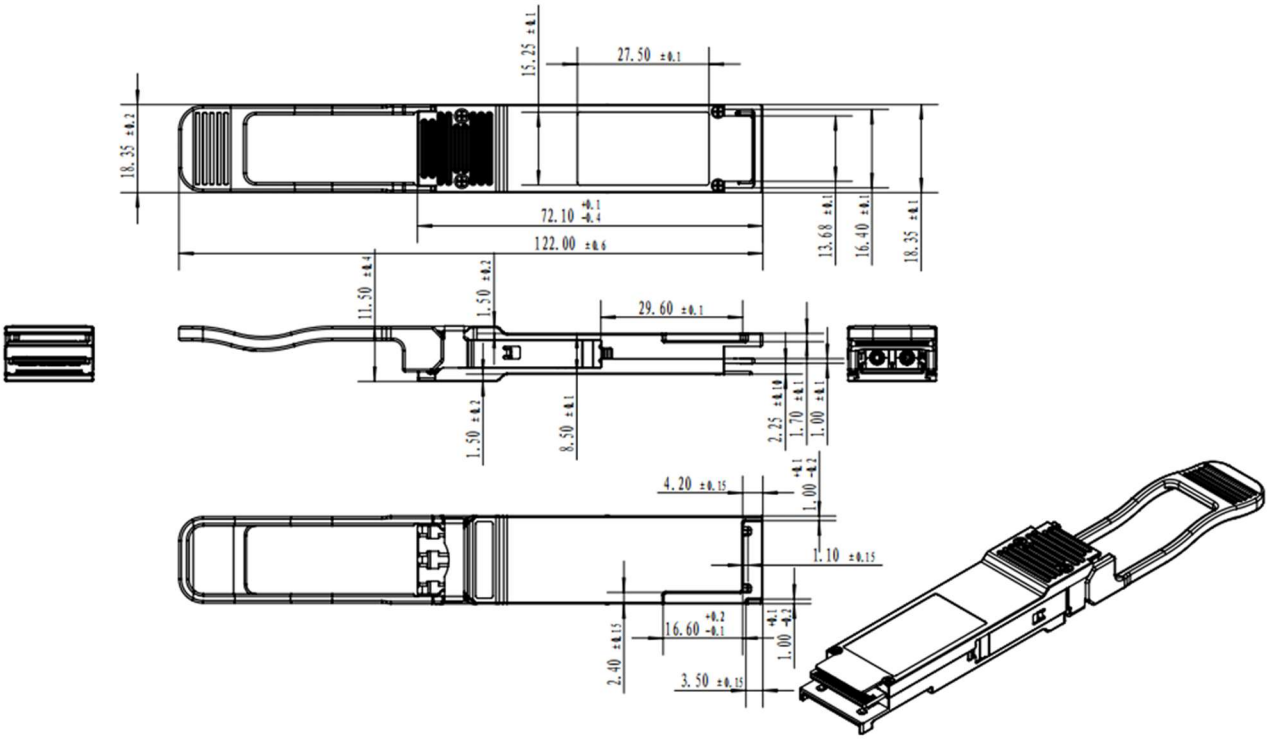
Recommended Power Supply Filter



Function Diagram



Mechanical Design Diagram



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate	Laser	Optical Power	Detector	Max Receiver Sensitivity	Temp.	Reach	Other	Application code
WST-QS28-DR-C	QSFP	Input 25.78 Gbps(NRZ)*4/ Optical 106.25 Gbps (PAM4)	1310nm EML	-2.9 ~ +4 dBm	PIN	max(−3.9,S_{ECQ}−5.3) dBm	0~70 °C	2 m to 500 m (with FEC)		100G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	29-Jan-2026	New Issue	Cynthia	Wayne	Wayne

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